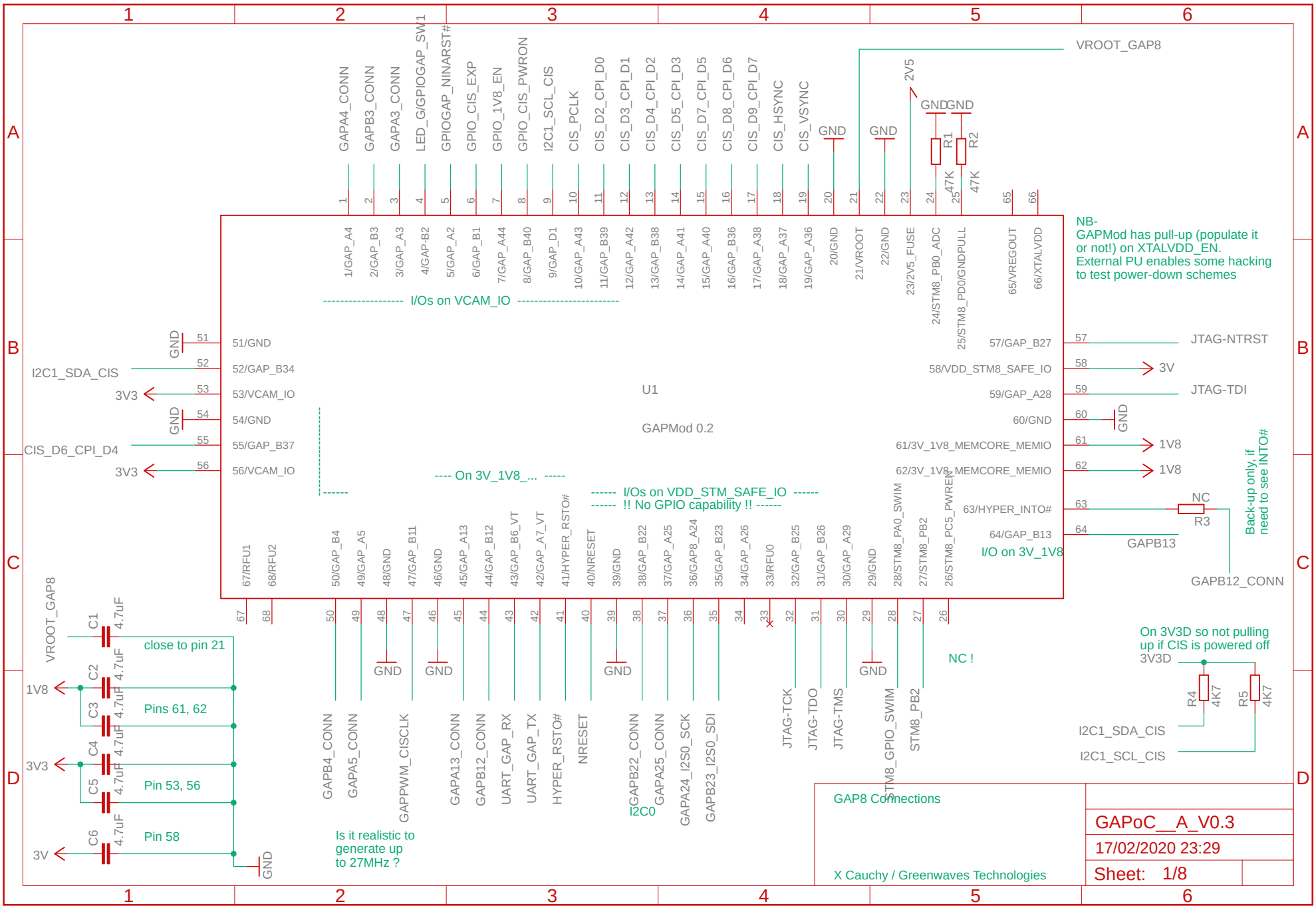
U1
GAPMod 0.2
GAPA4_CONN
GAPB3_CONN
GAPA3_CONN
LED_G/GPIOGAP_SW1
GPIOGAP_NINARST#
GPIO_CIS_EXP
GPIO_1V8_EN
GPIO_CIS_PWRON
I2C1_SCL_CIS
CIS_PCLK
CIS_D2_CPI_D0
CIS_D3_CPI_D1
CIS_D4_CPI_D2
CIS_D5_CPI_D3
CIS_D7_CPI_D5
CIS_D8_CPI_D6
CIS_D9_CPI_D7
CIS_HSYNC
CIS_VSYNC
GND
GND
2V5
GND
GND
R1
R2
47K
47K
VROOT_GAP8
1/GAP_A4
2/GAP_B3
3/GAP_A3
4/GAP-B2
5/GAP_A2
6/GAP_B1
7/GAP_A44
8/GAP_B40
9/GAP_D1
10/GAP_A43
11/GAP_B39
12/GAP_A42
13/GAP_B38
14/GAP_A41
15/GAP_A40
16/GAP_B36
17/GAP_A38
18/GAP_A37
19/GAP_A36
20/GND
21/VROOT
22/GND
23/2V5_FUSE
24/STM8_PB0_ADC
25/STM8_PD0/GNDPULL
65/VREGOUT
66/XTALVDD
I/Os on VCAM_IO
NB-
GAPMod has pull-up (populate it or not!) on XTALVDD_EN.
External PU enables some hacking to test power-down schemes
51/GND
52/GAP_B34
53/VCAM_IO
54/GND
55/GAP_B37
56/VCAM_IO
57/GAP_B27
58/VDD_STM8_SAFE_IO
59/GAP_A28
60/GND
61/3V_1V8_MEMCORE_MEMIO
62/3V_1V8_MEMCORE_MEMIO
63/HYPER_INTO#
64/GAP_B13
I/O on 3V_1V8
JTAG-NTRST
3V
JTAG-TDI
GND
1V8
1V8
NC
R3
GAPB13
GAPB12_CONN
Back-up only, if need to see INTO#
I2C1_SDA_CIS
3V3
3V3
GND
CIS_D6_CPI_D4
3V3
---- On 3V_1V8_... -----
------ I/Os on VDD_STM_SAFE_IO ------
------ !! No GPIO capability !! ------
67/RFU1
68/RFU2
50/GAP_B4
49/GAP_A5
48/GND
47/GAP_B11
46/GND
45/GAP_A13
44/GAP_B12
43/GAP_B6_VT
42/GAP_A7_VT
41/HYPER_RSTO#
40/NRESET
39/GND
38/GAP_B22
37/GAP_A25
36/GAP8_A24
35/GAP_B23
34/GAP_A26
33/RFU0
32/GAP_B25
31/GAP_B26
30/GAP_A29
29/GND
28/STM8_PA0_SWIM
27/STM8_PB2
26/STM8_PC5_PWREN
NC !
GND
GND
GND
GND
JTAG-TCK
JTAG-TDO
JTAG-TMS
GND
STM8_GPIO_SWIM
STM8_PB2
GAPB4_CONN
GAPA5_CONN
GAPPWM_CISCLK
GAPA13_CONN
GAPB12_CONN
UART_GAP_RX
UART_GAP_TX
HYPER_RSTO#
NRESET
GAPB22_CONN
GAPA25_CONN
GAPA24_I2S0_SCK
GAPB23_I2S0_SDI
I2C0
Is it realistic to generate up to 27MHz ?
VROOT_GAP8
C1
4.7uF
close to pin 21
1V8
C2
C3
4.7uF
4.7uF
Pins 61, 62
3V3
C4
C5
4.7uF
4.7uF
Pin 53, 56
3V
C6
4.7uF
Pin 58
GND
On 3V3D so not pulling up if CIS is powered off
3V3D
R4
4K7
R5
4K7
I2C1_SDA_CIS
I2C1_SCL_CIS
GAP8 Connections
X Cauchy / Greenwaves Technologies
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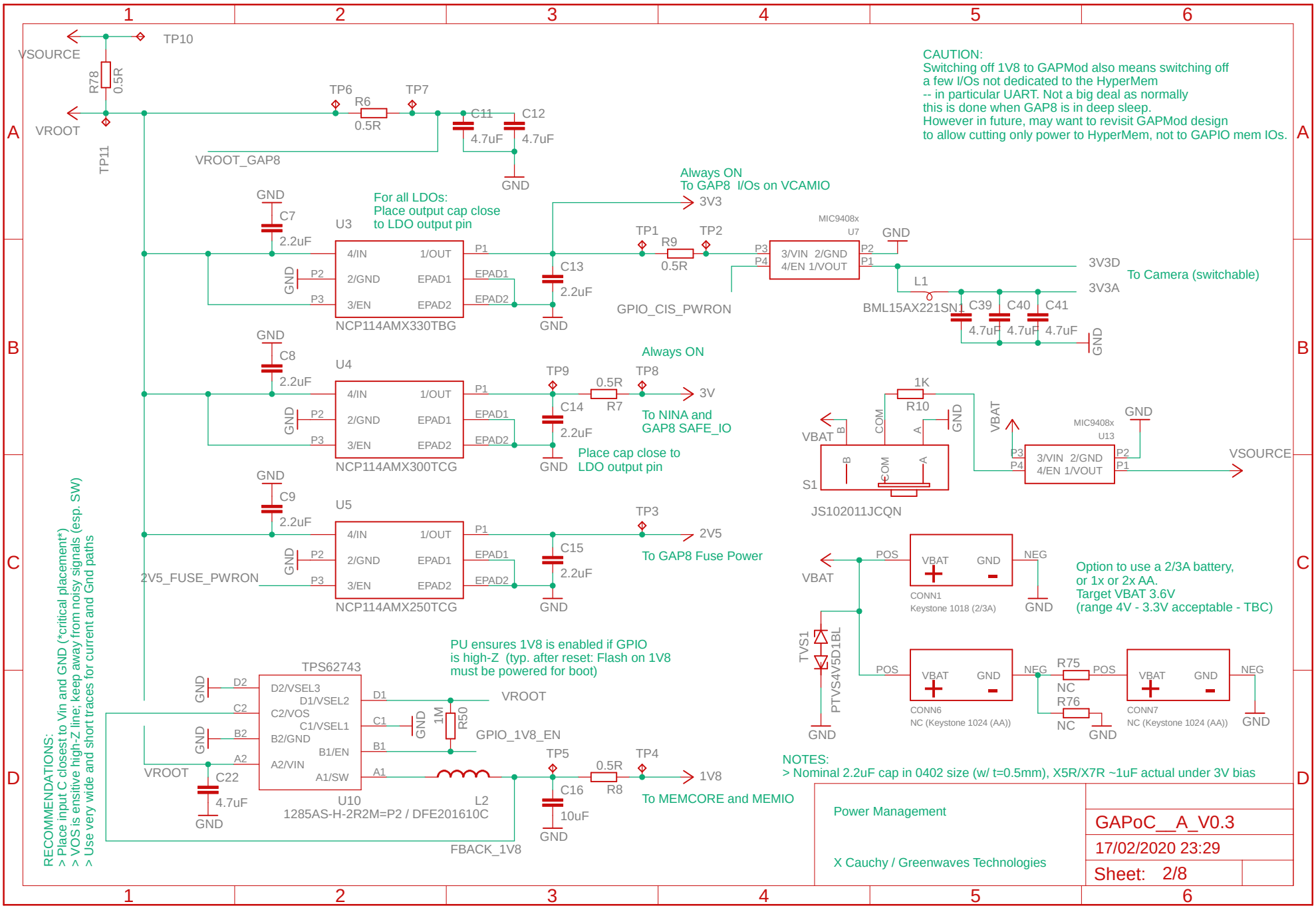
CAUTION:
Switching off 1V8 to GAPMod also means switching off
a few I/Os not dedicated to the HyperMem
-- in particular UART. Not a big deal as normally
this is done when GAP8 is in deep sleep.
However in future, may want to revisit GAPMod design
to allow cutting only power to HyperMem, not to GAPIO mem IOs.
VSOURCE
TP10
R78
0.5R
VROOT
TP11
TP6
R6
0.5R
TP7
C11
4.7uF
C12
4.7uF
VROOT_GAP8
GND
Always ON
To GAP8 I/Os on VCAMIO
3V3
For all LDOs:
Place output cap close
to LDO output pin
U3
C7
2.2uF
4/IN
2/GND
3/EN
1/OUT
EPAD1
EPAD2
P1
P2
P3
C13
2.2uF
NCP114AMX330TBG
TP1
R9
0.5R
TP2
GPIO_CIS_PWRON
MIC9408x
U7
3/VIN 2/GND
4/EN 1/VOUT
P3
P4
P2
P1
3V3D
3V3A
To Camera (switchable)
L1
BML15AX221SN1
C39
C40
C41
4.7uF
4.7uF
4.7uF
U4
C8
2.2uF
Always ON
TP9
0.5R
TP8
R7
3V
C14
2.2uF
To NINA and
GAP8 SAFE_IO
NCP114AMX300TCG
Place cap close to
LDO output pin
U5
C9
2.2uF
TP3
2V5
C15
2.2uF
To GAP8 Fuse Power
2V5_FUSE_PWRON
NCP114AMX250TCG
1K
R10
COM
A
B
VBAT
S1
JS102011JCQN
MIC9408x
U13
VSOURCE
PU ensures 1V8 is enabled if GPIO
is high-Z (typ. after reset: Flash on 1V8
must be powered for boot)
TPS62743
D2/VSEL3
D1/VSEL2
C2/VOS
C1/VSEL1
B2/GND
B1/EN
A2/VIN
A1/SW
D2
C2
B2
A2
D1
C1
B1
A1
1M
R50
GPIO_1V8_EN
VROOT
C22
4.7uF
U10
1285AS-H-2R2M=P2 / DFE201610C
L2
TP5
0.5R
TP4
R8
1V8
C16
10uF
To MEMCORE and MEMIO
FBACK_1V8
POS
NEG
CONN1
Keystone 1018 (2/3A)
Option to use a 2/3A battery,
or 1x or 2x AA.
Target VBAT 3.6V
(range 4V - 3.3V acceptable - TBC)
TVS1
PTVS4V5D1BL
R75
R76
NC
CONN6
NC (Keystone 1024 (AA))
CONN7
NC (Keystone 1024 (AA))
RECOMMENDATIONS:
> Place input C closest to Vin and GND (*critical placement*)
> VOS is ensitive high-Z line; keep away from noisy signals (esp. SW)
> Use very wide and short traces for current and Gnd paths
NOTES:
> Nominal 2.2uF cap in 0402 size (w/ t=0.5mm), X5R/X7R ~1uF actual under 3V bias
Power Management
X Cauchy / Greenwaves Technologies
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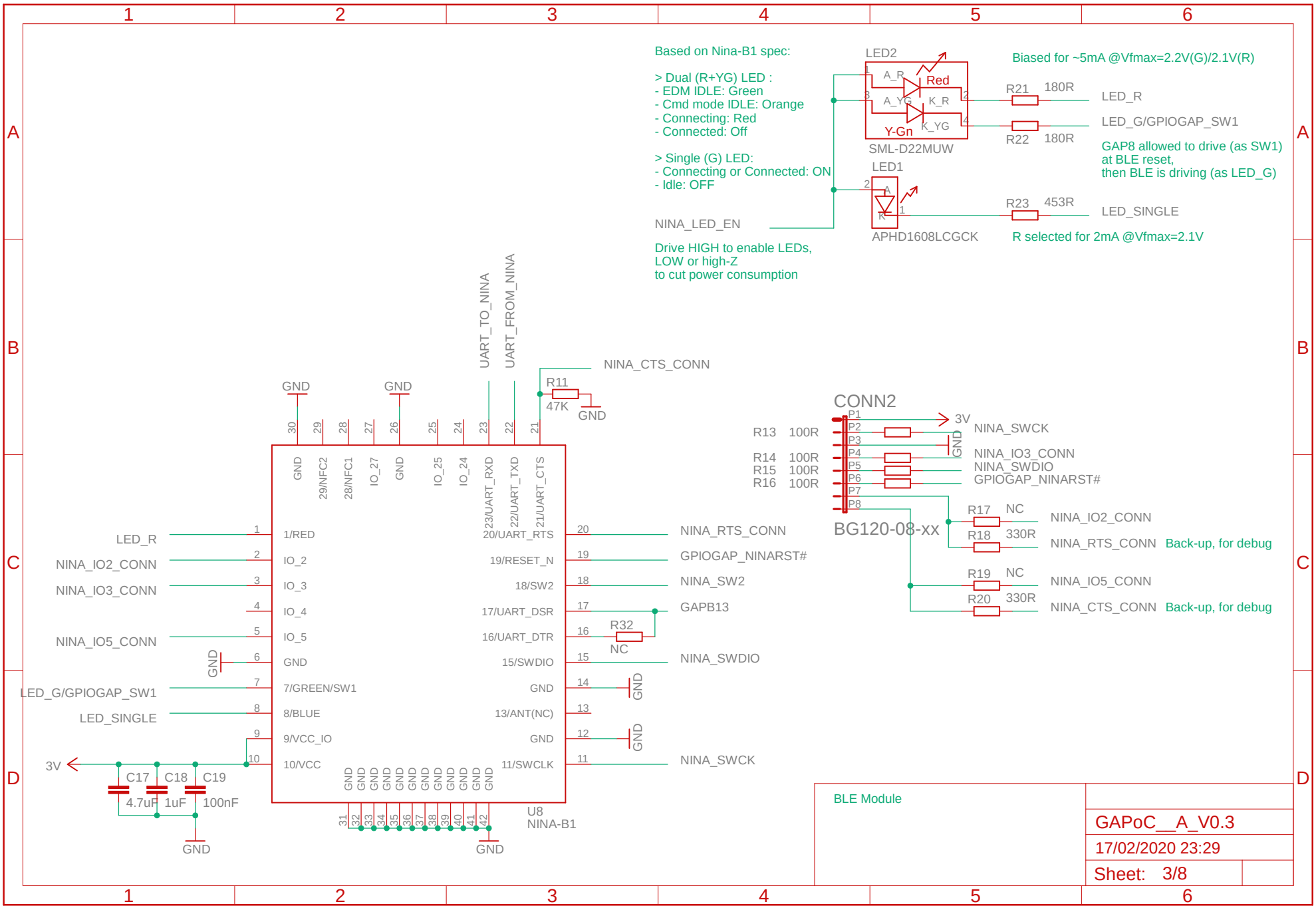
Based on Nina-B1 spec:
> Dual (R+YG) LED :
- EDM IDLE: Green
- Cmd mode IDLE: Orange
- Connecting: Red
- Connected: Off
> Single (G) LED:
- Connecting or Connected: ON
- Idle: OFF
NINA_LED_EN
Drive HIGH to enable LEDs, LOW or high-Z to cut power consumption
LED2
A_R
Red
A_YG
K_R
K_YG
Y-Gn
SML-D22MUW
LED1
APHD1608LCGCK
Biased for ~5mA @Vfmax=2.2V(G)/2.1V(R)
R21 180R
R22 180R
R23 453R
LED_R
LED_G/GPIOGAP_SW1
LED_SINGLE
GAP8 allowed to drive (as SW1) at BLE reset, then BLE is driving (as LED_G)
R selected for 2mA @Vfmax=2.1V
UART_TO_NINA
UART_FROM_NINA
NINA_CTS_CONN
R11 47K
GND
1/RED
IO_2
IO_3
IO_4
IO_5
GND
7/GREEN/SW1
8/BLUE
9/VCC_IO
10/VCC
20/UART_RTS
19/RESET_N
18/SW2
17/UART_DSR
16/UART_DTR
15/SWDIO
13/ANT(NC)
11/SWCLK
U8
NINA-B1
LED_R
NINA_IO2_CONN
NINA_IO3_CONN
NINA_IO5_CONN
LED_G/GPIOGAP_SW1
LED_SINGLE
3V
C17 4.7uF
C18 1uF
C19 100nF
NINA_RTS_CONN
GPIOGAP_NINARST#
NINA_SW2
GAPB13
R32 NC
NINA_SWDIO
NINA_SWCK
CONN2
BG120-08-xx
R13 100R
R14 100R
R15 100R
R16 100R
NINA_SWCK
NINA_IO3_CONN
NINA_SWDIO
GPIOGAP_NINARST#
R17 NC
R18 330R
R19 NC
R20 330R
NINA_IO2_CONN
NINA_RTS_CONN Back-up, for debug
NINA_IO5_CONN
NINA_CTS_CONN Back-up, for debug
BLE Module
GAPoC__A_V0.3
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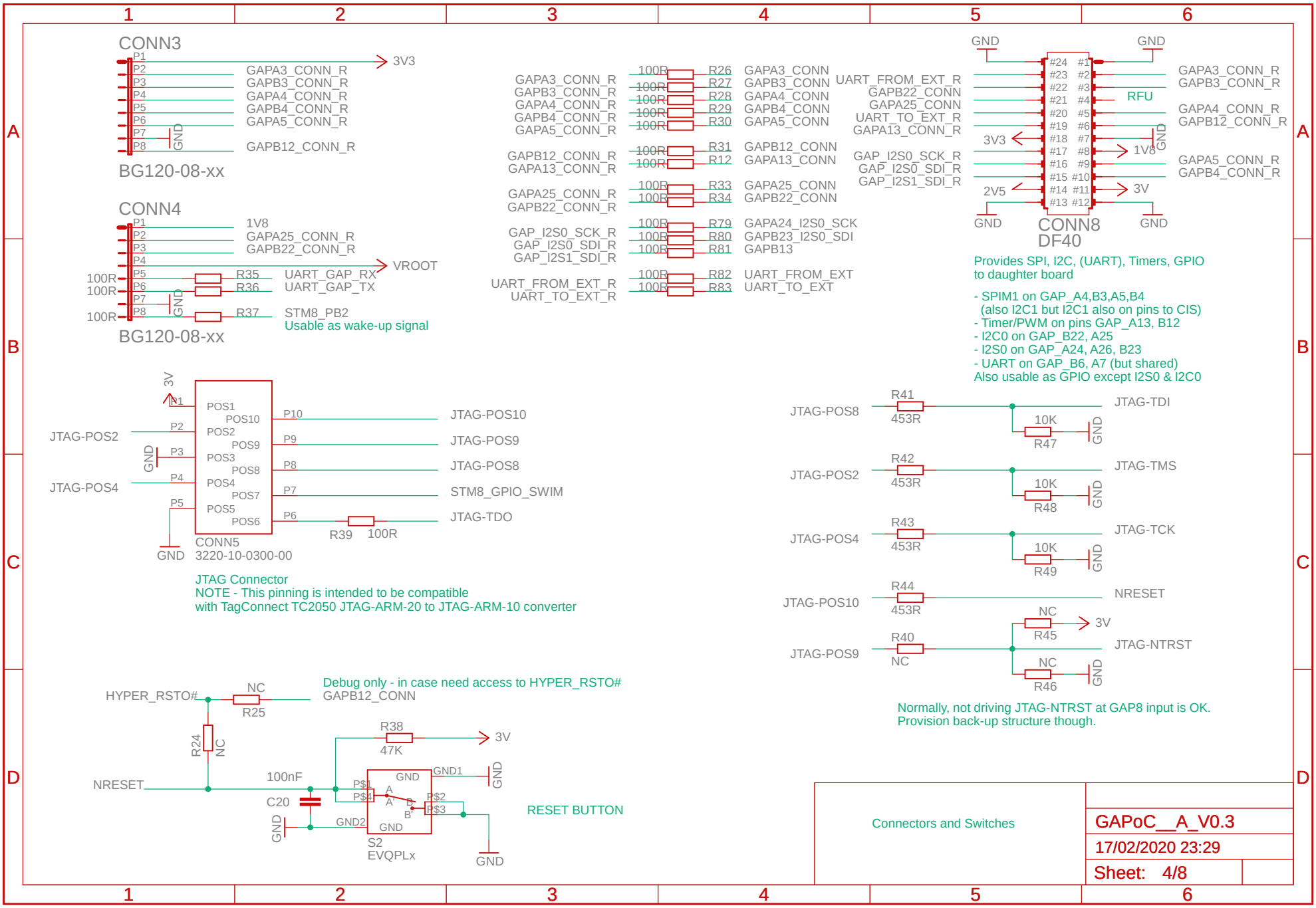
CONN3
P1
P2
P3
P4
P5
P6
P7
P8
GND
3V3
GAPA3_CONN_R
GAPB3_CONN_R
GAPA4_CONN_R
GAPB4_CONN_R
GAPA5_CONN_R
GAPB12_CONN_R
BG120-08-xx
CONN4
1V8
GAPA25_CONN_R
GAPB22_CONN_R
VROOT
100R
R35
R36
R37
UART_GAP_RX
UART_GAP_TX
STM8_PB2
Usable as wake-up signal
BG120-08-xx
GAPA3_CONN_R
GAPB3_CONN_R
GAPA4_CONN_R
GAPB4_CONN_R
GAPA5_CONN_R
GAPB12_CONN_R
GAPA13_CONN_R
GAPA25_CONN_R
GAPB22_CONN_R
GAP_I2S0_SCK_R
GAP_I2S0_SDI_R
GAP_I2S1_SDI_R
UART_FROM_EXT_R
UART_TO_EXT_R
R26
R27
R28
R29
R30
R31
R12
R33
R34
R79
R80
R81
R82
R83
GAPA3_CONN
GAPB3_CONN
GAPA4_CONN
GAPB4_CONN
GAPA5_CONN
GAPB12_CONN
GAPA13_CONN
GAPA25_CONN
GAPB22_CONN
GAPA24_I2S0_SCK
GAPB23_I2S0_SDI
GAPB13
UART_FROM_EXT
UART_TO_EXT
UART_FROM_EXT_R
GAPB22_CONN
GAPA25_CONN
UART_TO_EXT_R
GAPA13_CONN_R
GAP_I2S0_SCK_R
GAP_I2S0_SDI_R
GAP_I2S1_SDI_R
GND
GND
#24 #1
#23 #2
#22 #3
#21 #4
#20 #5
#19 #6
#18 #7
#17 #8
#16 #9
#15 #10
#14 #11
#13 #12
RFU
3V3
1V8
2V5
3V
GND
GND
GND
CONN8
DF40
GAPA3_CONN_R
GAPB3_CONN_R
GAPA4_CONN_R
GAPB12_CONN_R
GAPA5_CONN_R
GAPB4_CONN_R
Provides SPI, I2C, (UART), Timers, GPIO
to daughter board
- SPIM1 on GAP_A4,B3,A5,B4
(also I2C1 but I2C1 also on pins to CIS)
- Timer/PWM on pins GAP_A13, B12
- I2C0 on GAP_B22, A25
- I2S0 on GAP_A24, A26, B23
- UART on GAP_B6, A7 (but shared)
Also usable as GPIO except I2S0 & I2C0
3V
P1
P2
P3
P4
P5
POS1
POS10
POS2
POS9
POS3
POS8
POS4
POS7
POS5
POS6
P10
P9
P8
P7
P6
JTAG-POS2
JTAG-POS4
GND
GND
CONN5
3220-10-0300-00
R39
100R
JTAG-POS10
JTAG-POS9
JTAG-POS8
STM8_GPIO_SWIM
JTAG-TDO
JTAG Connector
NOTE - This pinning is intended to be compatible
with TagConnect TC2050 JTAG-ARM-20 to JTAG-ARM-10 converter
JTAG-POS8
JTAG-POS2
JTAG-POS4
JTAG-POS10
JTAG-POS9
R41
R42
R43
R44
R40
453R
10K
R47
R48
R49
R45
R46
NC
GND
3V
JTAG-TDI
JTAG-TMS
JTAG-TCK
NRESET
JTAG-NTRST
Normally, not driving JTAG-NTRST at GAP8 input is OK.
Provision back-up structure though.
HYPER_RSTO#
NC
R25
R24
NC
Debug only - in case need access to HYPER_RSTO#
GAPB12_CONN
R38
47K
3V
NRESET
100nF
C20
GND
GND2
GND
GND1
GND
GND
P$1
P$4
P$2
P$3
A
A'
B
B'
S2
EVQPLx
RESET BUTTON
Connectors and Switches
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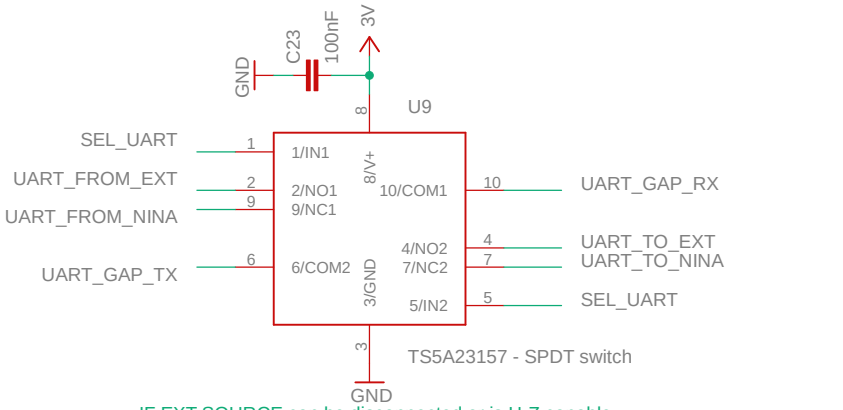
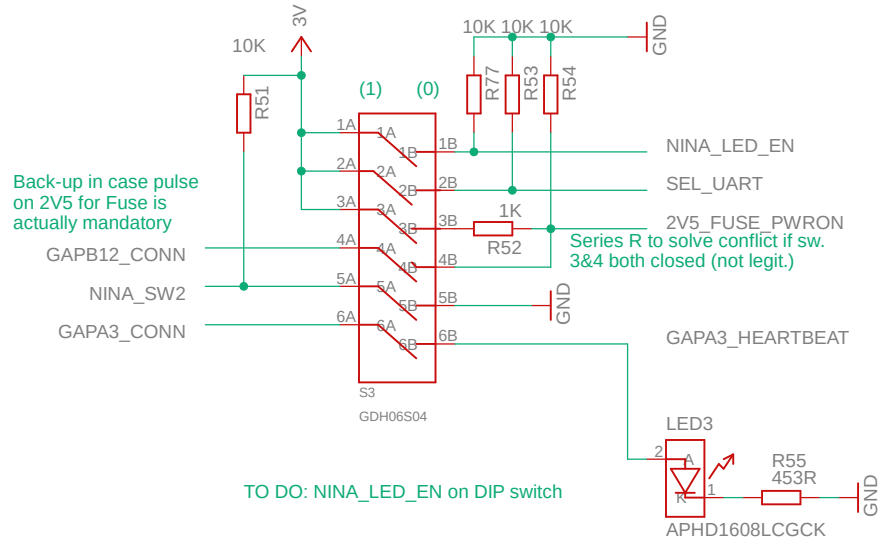
Issue if wired-ANDing HYPER_RSTO# with NRESET
and switching off 1V8 from GAP8 GPIO:
would cause assertion of HYPER_RSTO#
hence of NRESET and therefore reset of GAP8 !



IF EXT SOURCE can be disconnected or is H-Z capable,
then CONNx can be used not only as TP but also to plug UART i/f to talk with GAP8

NB:
-Slight static power consumption when switch is closed (3V/10K=300uA)
- Default switch position = (0) / Open - for normal use case

Open/closed switches :
1: n/a
2: selects UART for NINA or for Conn.
3: selects if Fuse Power Enable is Off/forced on
4: selects if Fuse Power Enable is controlled from GPIO
(dont select ForcedOn + GPIO-based)
5: selects normal or bootload/restore modes at NINA startup
6: selects if GAP_A3 is available as GPIO on connector
or is recycled as heartbeat LED



TO DO: NINA_LED_EN on DIP switch

One non-plated hole in each corner

H1 MOUNT-HOLE-2.8
H2 MOUNT-HOLE-2.8
H3 MOUNT-HOLE-2.8
H4 MOUNT-HOLE-2.8

Fiducials

Switches & Electro-mechanics

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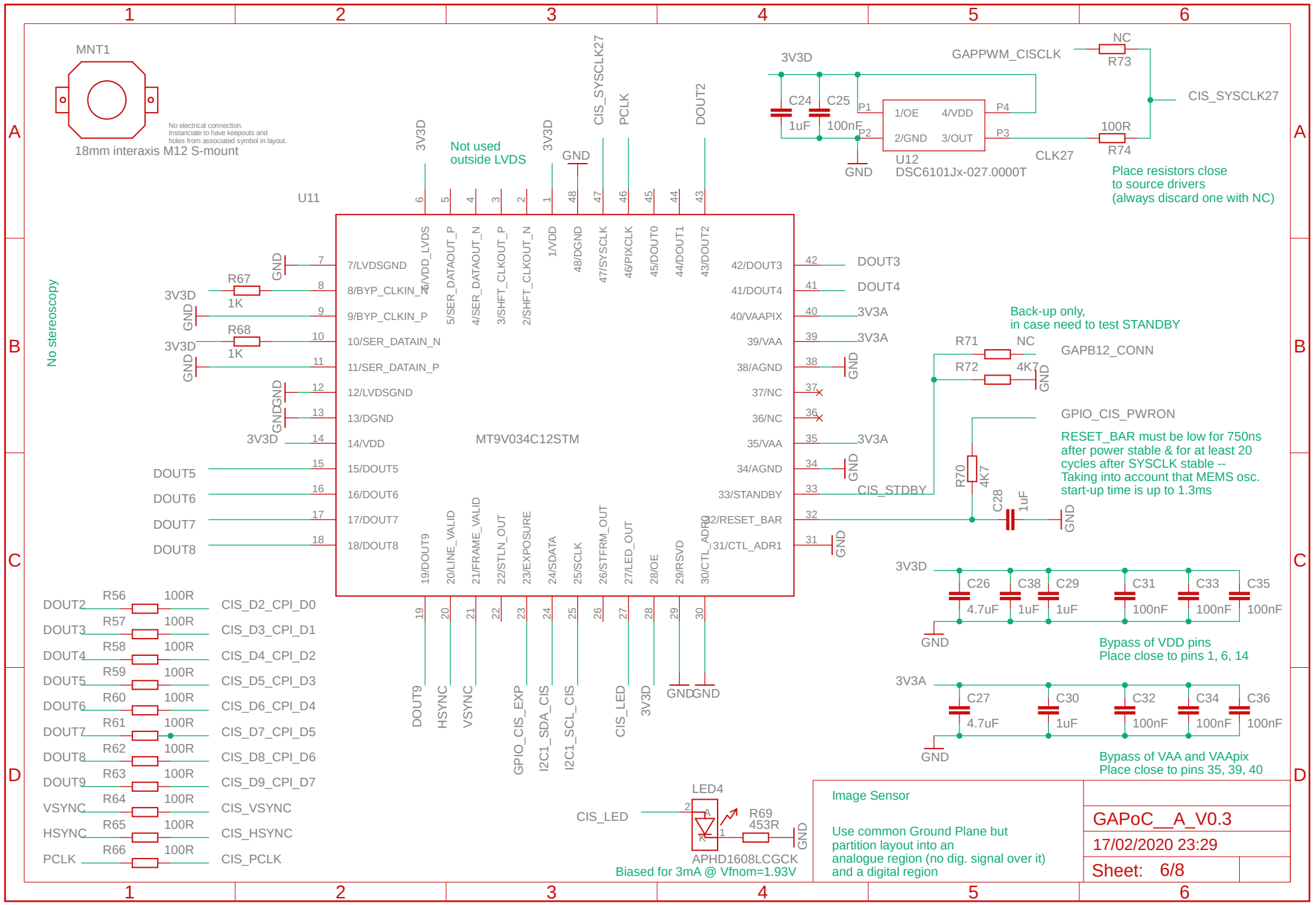
MNT1
18mm interaxis M12 S-mount
No electrical connection.
Instanciate to have keepouts and
holes from associated symbol in layout.
U11
MT9V034C12STM
Not used
outside LVDS
No stereoscopy
3V3D
GND
CIS_SYSCLK27
PCLK
DOUT2
DOUT3
DOUT4
DOUT5
DOUT6
DOUT7
DOUT8
DOUT9
HSYNC
VSYNC
GPIO_CIS_EXP
I2C1_SDA_CIS
I2C1_SCL_CIS
CIS_LED
7/LVDSGND
8/BYP_CLKIN_N
9/BYP_CLKIN_P
10/SER_DATAIN_N
11/SER_DATAIN_P
12/LVDSGND
13/DGND
14/VDD
15/DOUT5
16/DOUT6
17/DOUT7
18/DOUT8
19/DOUT9
20/LINE_VALID
21/FRAME_VALID
22/STLN_OUT
23/EXPOSURE
24/SDATA
25/SCLK
26/STFRM_OUT
27/LED_OUT
28/OE
29/RSVD
30/CTL_ADR3
31/CTL_ADR1
32/RESET_BAR
33/STANDBY
34/AGND
35/VAA
36/NC
37/NC
38/AGND
39/VAA
40/VAAPIX
41/DOUT4
42/DOUT3
43/DOUT2
44/DOUT1
45/DOUT0
46/PIXCLK
47/SYSCLK
48/DGND
1/VDD
2/SHFT_CLKOUT_N
3/SHFT_CLKOUT_P
4/SER_DATAOUT_N
5/SER_DATAOUT_P
6/VDD_LVDS
R67 1K
R68 1K
R56 100R CIS_D2_CPI_D0
R57 100R CIS_D3_CPI_D1
R58 100R CIS_D4_CPI_D2
R59 100R CIS_D5_CPI_D3
R60 100R CIS_D6_CPI_D4
R61 100R CIS_D7_CPI_D5
R62 100R CIS_D8_CPI_D6
R63 100R CIS_D9_CPI_D7
R64 100R CIS_VSYNC
R65 100R CIS_HSYNC
R66 100R CIS_PCLK
U12
DSC6101Jx-027.0000T
1/OE
2/GND
3/OUT
4/VDD
P1
P2
P3
P4
C24 1uF
C25 100nF
GAPPWM_CISCLK
NC
R73
100R
R74
CLK27
Place resistors close
to source drivers
(always discard one with NC)
Back-up only,
in case need to test STANDBY
R71 NC
R72 4K7
GAPB12_CONN
GPIO_CIS_PWRON
RESET_BAR must be low for 750ns
after power stable & for at least 20
cycles after SYSCLK stable --
Taking into account that MEMS osc.
start-up time is up to 1.3ms
R70 4K7
C28 1uF
CIS_STDBY
C26 4.7uF
C38 1uF
C29 1uF
C31 100nF
C33 100nF
C35 100nF
Bypass of VDD pins
Place close to pins 1, 6, 14
C27 4.7uF
C30 1uF
C32 100nF
C34 100nF
C36 100nF
Bypass of VAA and VAApix
Place close to pins 35, 39, 40
LED4
APHD1608LCGCK
R69 453R
Biased for 3mA @ Vfnom=1.93V
A voir:
better solution than just truncating
by dropping 2 LSBs from CIS ???
Image Sensor
Use common Ground Plane but
partition layout into an
analogue region (no dig. signal over it)
and a digital region
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