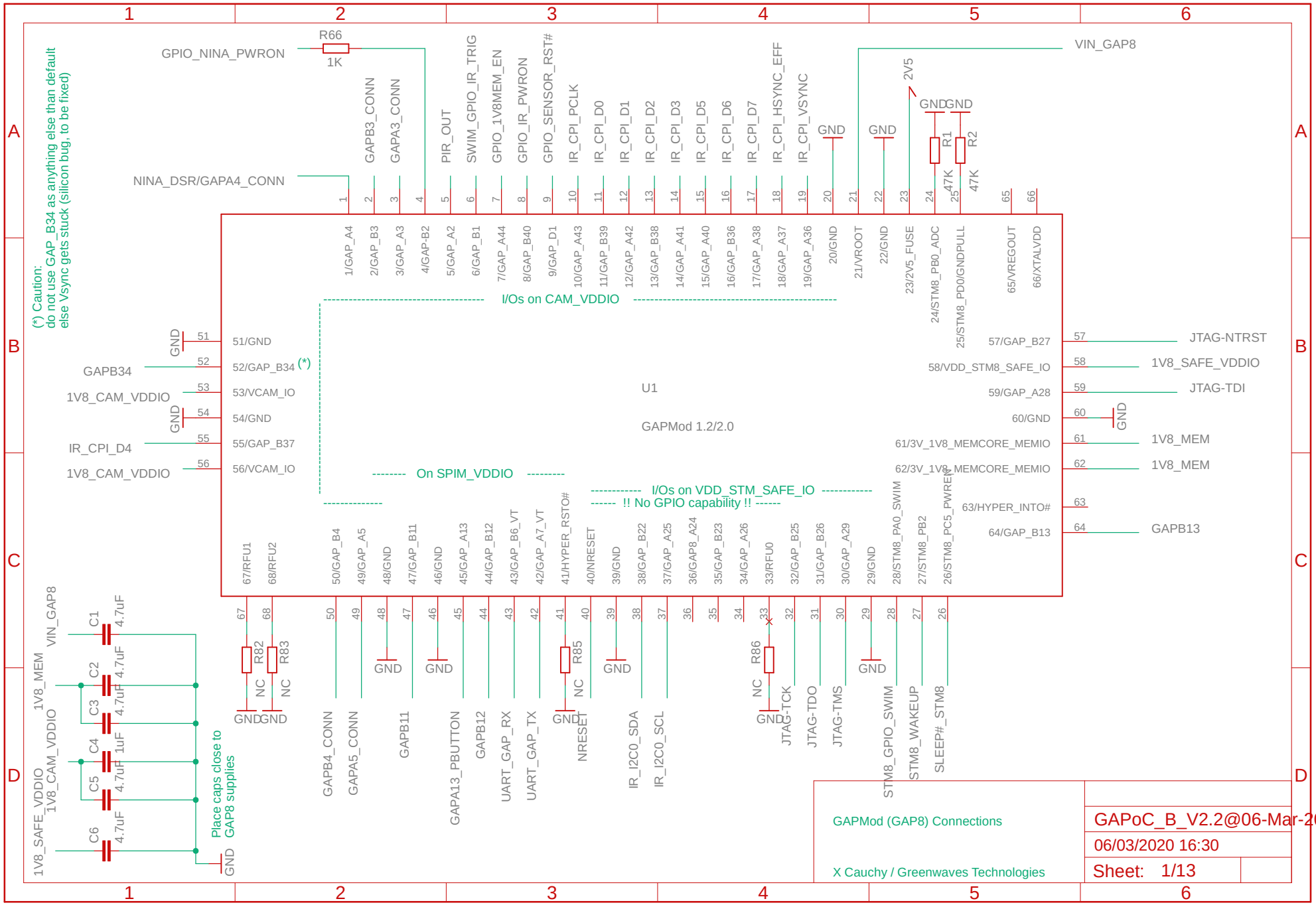
(*) Caution:
do not use GAP_B34 as anything else than default
else Vsync gets stuck (silicon bug, to be fixed)
U1
GAPMod 1.2/2.0
I/Os on CAM_VDDIO
On SPIM_VDDIO
I/Os on VDD_STM_SAFE_IO
!! No GPIO capability !!
GPIO_NINA_PWRON
R66
1K
NINA_DSR/GAPA4_CONN
GAPB3_CONN
GAPA3_CONN
PIR_OUT
SWIM_GPIO_IR_TRIG
GPIO_1V8MEM_EN
GPIO_IR_PWRON
GPIO_SENSOR_RST#
IR_CPI_PCLK
IR_CPI_D0
IR_CPI_D1
IR_CPI_D2
IR_CPI_D3
IR_CPI_D5
IR_CPI_D6
IR_CPI_D7
IR_CPI_HSYNC_EFF
IR_CPI_VSYNC
VIN_GAP8
2V5
R1
R2
47K
GAPB34
1V8_CAM_VDDIO
IR_CPI_D4
JTAG-NTRST
1V8_SAFE_VDDIO
JTAG-TDI
1V8_MEM
GAPB13
R82
R83
R85
R86
NC
GAPB4_CONN
GAPA5_CONN
GAPB11
GAPA13_PBUTTON
GAPB12
UART_GAP_RX
UART_GAP_TX
NRESET
IR_I2C0_SDA
IR_I2C0_SCL
JTAG-TCK
JTAG-TDO
JTAG-TMS
STM8_GPIO_SWIM
STM8_WAKEUP
SLEEP#_STM8
C1
C2
C3
C4
C5
C6
4.7uF
1uF
Place caps close to
GAP8 supplies
GAPMod (GAP8) Connections
X Cauchy / Greenwaves Technologies
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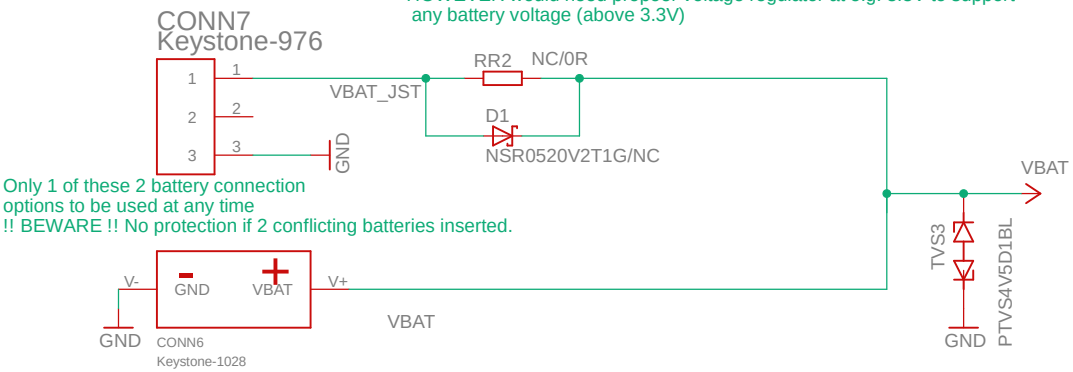
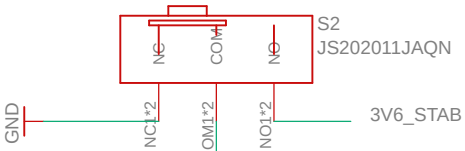
NOTE: IR Sensor requires a stable VDDA @3.6V nom/max, 3.5V min.
Supported battery options are as follows:
> Option 1: single 3.6V SAFT-type primary battery, normally in on-board AA holder
Voltage of battery can go down to ~3.3-3.4V when drawing significant current so need boost conv
> Option 2: external battery holder through JST connector
With this implementation external voltage must NOT EXCEED 3.6V, or 3.8V with D1 schottky diode implemented
-- to make sure no more than 3.6V reaches VIN_DCDC input of GAP8
Minimum required voltage for proper operation is 2.8V (without D1 schottky) or 3V (with D1 Schottky).
BEWARE: 3xNiMh at nominal votlage = 3x1.2=3.6V, which would be OK;
HOWEVER a fully charged NiMH cell can reach 1.3-1.4 so that 3x NiMH at full charge ~ 4V-4.2 which is too much and may damage parts !!

Optional (assy option) Schottky diode allows to accept voltages slightly above 3.6V (up to ~3.8V) to ease support of external batteries
HOWEVER would need propoer voltage regulator at e.g. 3.3V to support any battery voltage (above 3.3V)

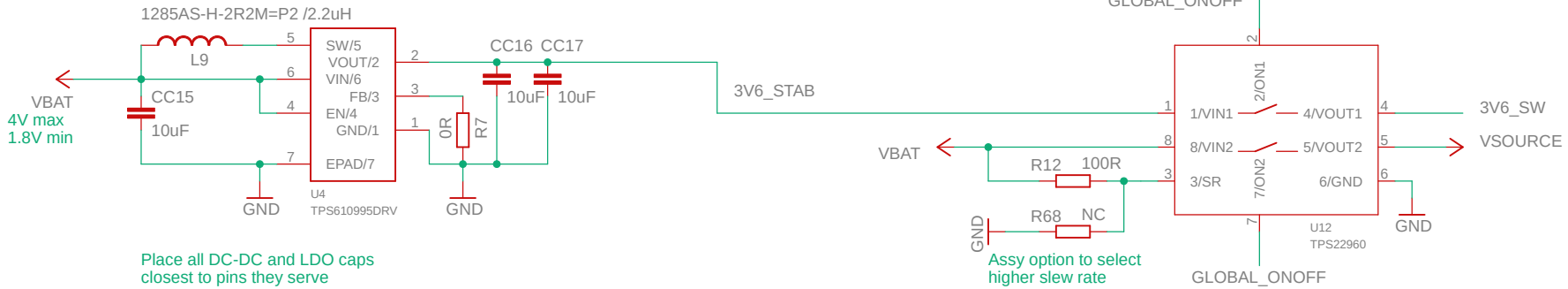


BATTERY HOLDERS/CONNECTORS

BOARD ON/OFF SWITCH



Note 2:
BoostConv kept upstream of global ON/OFF switch for legacy reasons.
Selected Boost Conv is ultra-low IDDq (1uA) so not too much of an issue re. current draw on battery.
Could be moved downstream of ON/OFF switch in future evolution.



Place all DC-DC and LDO caps closest to pins they serve

BATTERIES & MASTER POWER

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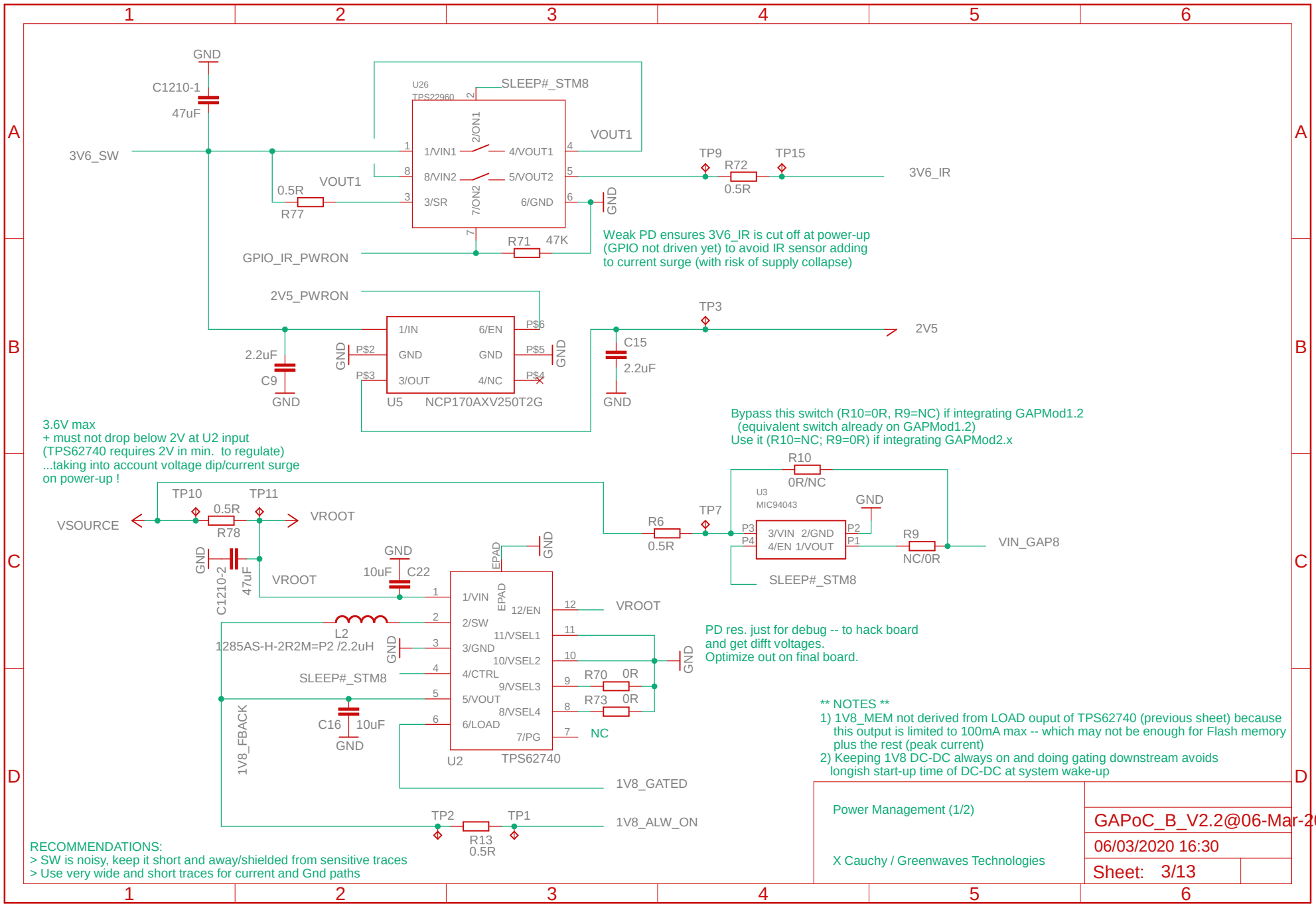
GND
C1210-1
47uF
3V6_SW
U26
TPS22960
SLEEP#_STM8
2/ON1
VOUT1
1/VIN1
4/VOUT1
8/VIN2
5/VOUT2
3/SR
7/ON2
6/GND
TP9
TP15
R72
0.5R
3V6_IR
0.5R
R77
VOUT1
GND
R71
47K
GPIO_IR_PWRON
Weak PD ensures 3V6_IR is cut off at power-up
(GPIO not driven yet) to avoid IR sensor adding
to current surge (with risk of supply collapse)
2V5_PWRON
TP3
2V5
1/IN
6/EN
GND
GND
3/OUT
4/NC
P$2
P$3
P$4
P$5
P$6
2.2uF
C9
C15
2.2uF
U5
NCP170AXV250T2G
3.6V max
+ must not drop below 2V at U2 input
(TPS62740 requires 2V in min. to regulate)
...taking into account voltage dip/current surge
on power-up !
Bypass this switch (R10=0R, R9=NC) if integrating GAPMod1.2
(equivalent switch already on GAPMod1.2)
Use it (R10=NC; R9=0R) if integrating GAPMod2.x
R10
0R/NC
U3
MIC94043
TP7
R6
0.5R
3/VIN 2/GND
4/EN 1/VOUT
R9
NC/0R
VIN_GAP8
SLEEP#_STM8
TP10
TP11
0.5R
R78
VSOURCE
VROOT
C1210-2
47uF
10uF
C22
EPAD
1/VIN
12/EN
2/SW
11/VSEL1
3/GND
10/VSEL2
4/CTRL
9/VSEL3
5/VOUT
8/VSEL4
6/LOAD
7/PG
L2
1285AS-H-2R2M=P2 /2.2uH
SLEEP#_STM8
R70
R73
0R
NC
C16
10uF
1V8_FBACK
U2
TPS62740
1V8_GATED
PD res. just for debug -- to hack board
and get difft voltages.
Optimize out on final board.
** NOTES **
1) 1V8_MEM not derived from LOAD ouput of TPS62740 (previous sheet) because
this output is limited to 100mA max -- which may not be enough for Flash memory
plus the rest (peak current)
2) Keeping 1V8 DC-DC always on and doing gating downstream avoids
longish start-up time of DC-DC at system wake-up
TP2
TP1
R13
0.5R
1V8_ALW_ON
RECOMMENDATIONS:
> SW is noisy, keep it short and away/shielded from sensitive traces
> Use very wide and short traces for current and Gnd paths
Power Management (1/2)
X Cauchy / Greenwaves Technologies
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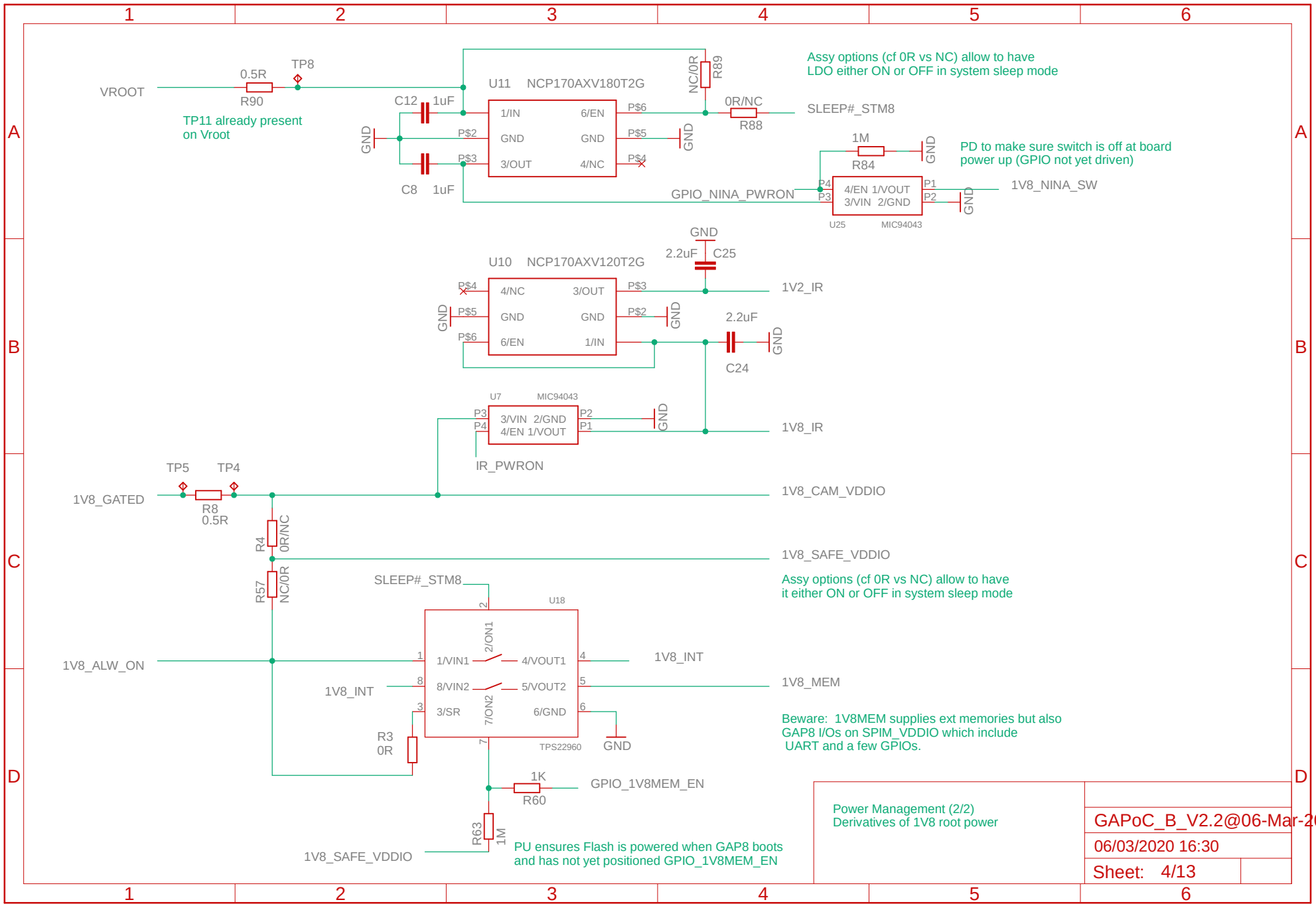
VROOT
0.5R
R90
TP8
TP11 already present on Vroot
C12 1uF
C8 1uF
GND
U11 NCP170AXV180T2G
1/IN
GND
3/OUT
6/EN
GND
4/NC
P$2
P$3
P$6
P$5
P$4
NC/0R
R89
0R/NC
R88
SLEEP#_STM8
Assy options (cf 0R vs NC) allow to have LDO either ON or OFF in system sleep mode
1M
R84
PD to make sure switch is off at board power up (GPIO not yet driven)
GPIO_NINA_PWRON
4/EN 1/VOUT
3/VIN 2/GND
U25 MIC94043
1V8_NINA_SW
U10 NCP170AXV120T2G
2.2uF C25
1V2_IR
2.2uF
C24
1V8_IR
U7 MIC94043
3/VIN 2/GND
4/EN 1/VOUT
IR_PWRON
TP5 TP4
1V8_GATED
R8 0.5R
1V8_CAM_VDDIO
R4 0R/NC
R57 NC/0R
1V8_SAFE_VDDIO
Assy options (cf 0R vs NC) allow to have it either ON or OFF in system sleep mode
U18
2/ON1
1/VIN1
4/VOUT1
1V8_ALW_ON
1V8_INT
8/VIN2
5/VOUT2
1V8_MEM
3/SR
7/ON2
6/GND
TPS22960
R3 0R
Beware: 1V8MEM supplies ext memories but also GAP8 I/Os on SPIM_VDDIO which include UART and a few GPIOs.
1K
R60
GPIO_1V8MEM_EN
R63 1M
PU ensures Flash is powered when GAP8 boots and has not yet positioned GPIO_1V8MEM_EN
Power Management (2/2)
Derivatives of 1V8 root power
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NOTE on LEDs :
I/Os controlling LEDs are 0V-1V8 while Vf of LED is ~1.8v-2V.
In this design, applying 2.5V on anode and controlling cathode from I/O, so that:
- LED ON when I/Os is 0V.
- LED Off when I/O driven to either Logic1 (1.8V) or (better) High-Z
Some small current might still circulate in OFF mode,
but not enough to light LED (or perhaps, if applying 1 Logic1 rather than High-Z, extremely dim).
Not an issue from power perspective as only used in debug mode
(2V5 can be switched off in normal mode)
[Also applies to other 2V5-powered LEDs used in this design]

Using difft LED color scheme vs. Nina spec

Biased for I~2mA

LED2
A_R
Red
A_YG
K_R
Y-Gn
K_YG
SML-D22MUW
R21 330R
R22 330R
LED_R
GND
LED_G always on if LEDs enabled

Switchable 2V5 (cf DIP Switch)
Turn on for debug/bring-up,
off to save power

LED1
APHD1608LCGCK
R23 330R
LED_SINGLE
2V5_LED

NB - Nina will driving I/O to Logic1=1.8V will mean LED off.
At this point stil 2.5-1.8=0.7V across LED --
not strictly off but not sufficient for LED to shine

UART_TO_NINA
UART_FROM_NINA
R11 47K
GND

U8
NINA-B1
GND
29/NFC2
28/NFC1
IO_27
IO_25
IO_24
23/UART_RXD
22/UART_TXD
21/UART_CTS
1/RED
IO_2
IO_3
IO_4
IO_5
7/GREEN/SW1
8/BLUE
9/VCC_IO
10/VCC
20/UART_RTS
19/RESET_N
18/SW2
17/UART_DSR
16/UART_DTR
15/SWDIO
13/ANT(NC)
11/SWCLK
LED_R
NINA_SW1/2
LED_SINGLE
1V8_NINA_SW
(internal PU)
NINA_RST#
R103 0R
NINA_SW1/2
R24 0R
NINA_DSR/GAPA4_CONN
NC R32
SWDIO
SWCLK
C17 4.7uF
C18 1uF
C19 100nF

NB - Allowing control of GPIO_NINA_PWRON
from here to force enable of
NINA's VDD when programming thru SWD

1V8_NINA_SW
SWCLK
SWDIO
CONN2
TC2030-IDC-NL Footprint
GPIO_NINA_PWRON
NINA_RST#

Usage of NINA_DSR (typ. for NINA deep sleep)
exclusive with usage of GAP_A4 on connector
-- in particular, exclusive w/ usage of SPI MISO
of LCD possibly connected to SPI on conn.
Not a big problem as trying to minimie Niina power
(deep sleep) while using power-hungry LCD
wouldn't make much sense...

BLE Module

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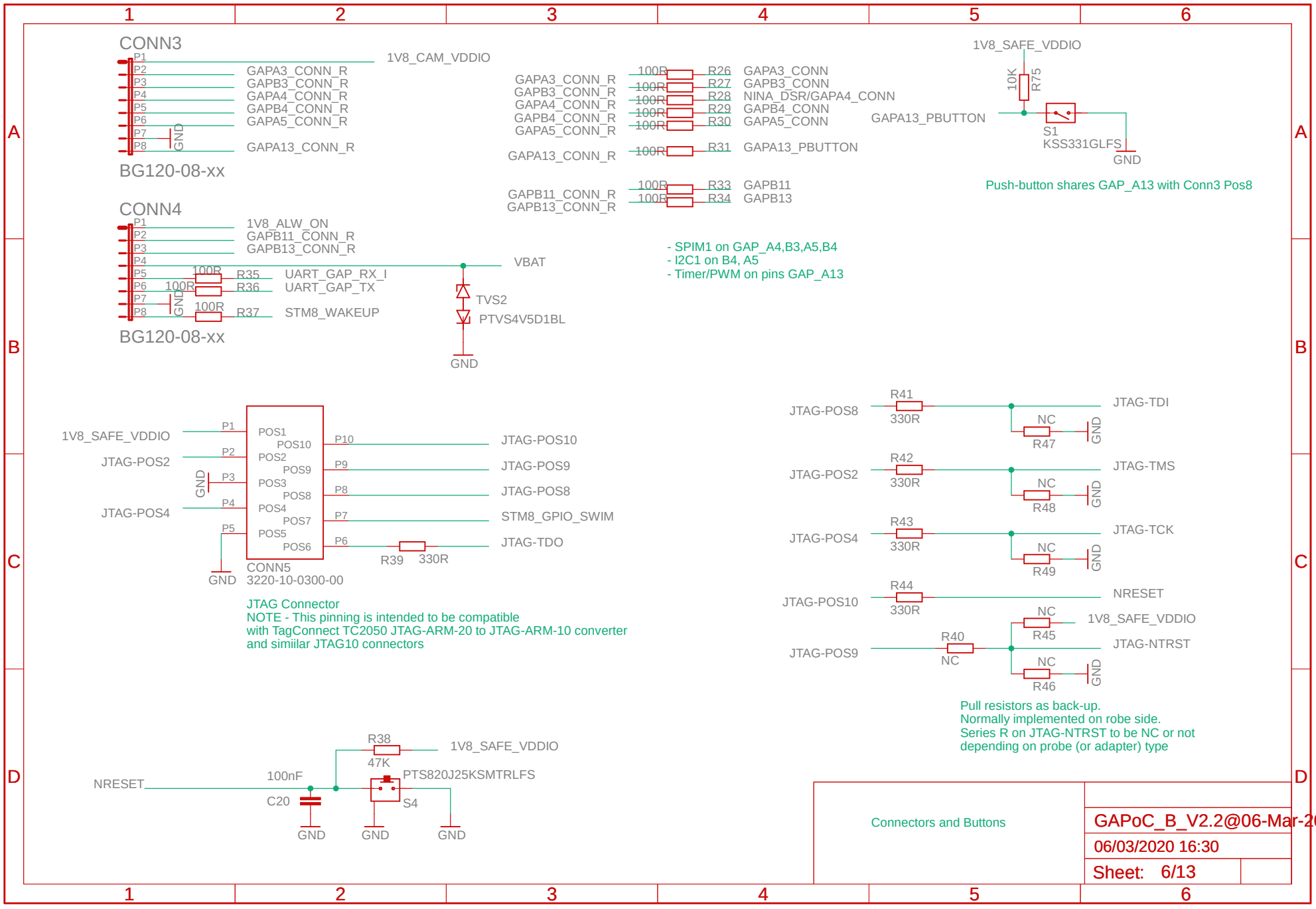
CONN3
P1
P2
P3
P4
P5
P6
P7
P8
GND
1V8_CAM_VDDIO
GAPA3_CONN_R
GAPB3_CONN_R
GAPA4_CONN_R
GAPB4_CONN_R
GAPA5_CONN_R
GAPA13_CONN_R
BG120-08-xx
CONN4
1V8_ALW_ON
GAPB11_CONN_R
GAPB13_CONN_R
100R
R35
R36
R37
UART_GAP_RX_I
UART_GAP_TX
STM8_WAKEUP
VBAT
TVS2
PTVS4V5D1BL
BG120-08-xx
GAPA3_CONN_R
GAPB3_CONN_R
GAPA4_CONN_R
GAPB4_CONN_R
GAPA5_CONN_R
GAPA13_CONN_R
GAPB11_CONN_R
GAPB13_CONN_R
R26
R27
R28
R29
R30
R31
R33
R34
GAPA3_CONN
GAPB3_CONN
NINA_DSR/GAPA4_CONN
GAPB4_CONN
GAPA5_CONN
GAPA13_PBUTTON
GAPB11
GAPB13
- SPIM1 on GAP_A4,B3,A5,B4
- I2C1 on B4, A5
- Timer/PWM on pins GAP_A13
1V8_SAFE_VDDIO
10K
R75
S1
KSS331GLFS
GND
Push-button shares GAP_A13 with Conn3 Pos8
1V8_SAFE_VDDIO
JTAG-POS2
JTAG-POS4
JTAG-POS10
JTAG-POS9
JTAG-POS8
STM8_GPIO_SWIM
JTAG-TDO
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
POS1
POS2
POS3
POS4
POS5
POS6
POS7
POS8
POS9
POS10
R39
330R
CONN5
3220-10-0300-00
JTAG Connector
NOTE - This pinning is intended to be compatible
with TagConnect TC2050 JTAG-ARM-20 to JTAG-ARM-10 converter
and simiilar JTAG10 connectors
JTAG-POS8
JTAG-POS2
JTAG-POS4
JTAG-POS10
JTAG-POS9
R41
R42
R43
R44
R40
330R
NC
R47
R48
R49
R45
R46
JTAG-TDI
JTAG-TMS
JTAG-TCK
NRESET
1V8_SAFE_VDDIO
JTAG-NTRST
Pull resistors as back-up.
Normally implemented on robe side.
Series R on JTAG-NTRST to be NC or not
depending on probe (or adapter) type
NRESET
R38
47K
100nF
C20
PTS820J25KSMTRLFS
S4
1V8_SAFE_VDDIO
Connectors and Buttons
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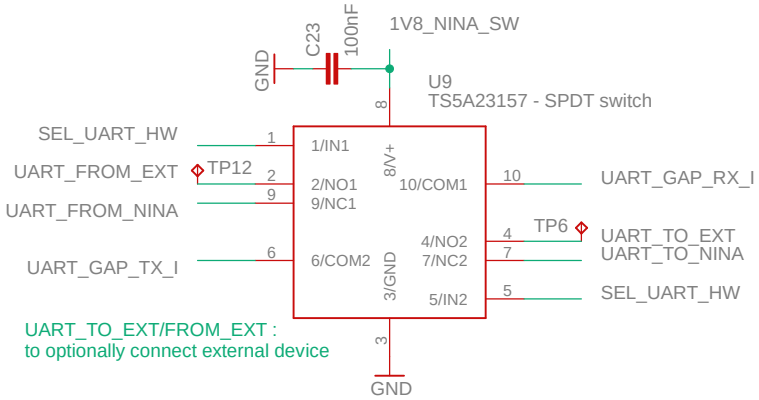
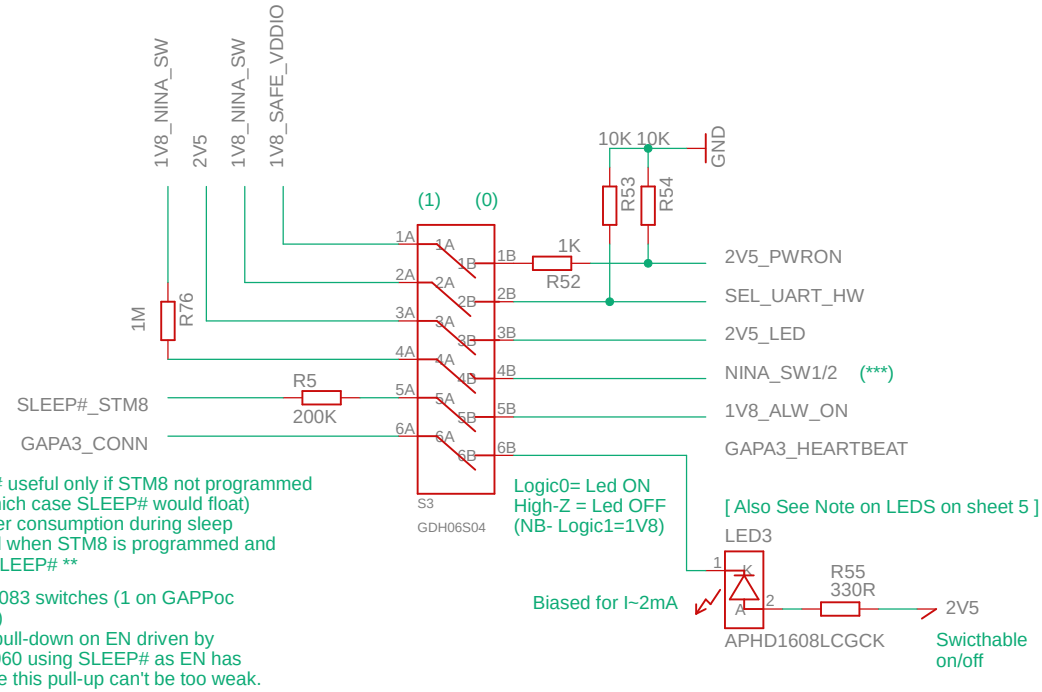
** This could be optimized out **
Dropping UART_TO_EXT, UART_FROM_EXT.
Keeping just UART for Nina (and CONN4)



UART_TO_EXT/FROM_EXT :
to optionally connect external device

Caution:
when 1V8_Nina_Sw is switched off,
GAP8 must drive UART_GAP_TX to Logic0
to avoid excessive power consumption

Open/closed switches :
1: close to provide 2V5 to VQPS pin (Fuse prog.) and to on-board LEDs
2: select if GAP8's UART talks with NINA (open) or with external UART (closed)
3: close to enable status LEDs of NINA & IR sensor (which will draw a few mA)
4: close for nomal boot of Nina
5: close to pull SLEEP# at start-up (required if STM8 not programmed), open to minimize static current
6: close to enable User LED, open to keep A3 available



Pull-up on SLEEP# useful only if STM8 not programmed
/ not present (in which case SLEEP# would float)
Causes ~9uA power consumption during sleep
** Can be removed when STM8 is programmed and
properly controls SLEEP# **

Beware - 2 MIC94083 switches (1 on GAPPoc
and 1 on GAPMod)
have weak (~2M) pull-down on EN driven by
SLEEP# + TPS22960 using SLEEP# as EN has
VIH=1.4V; therefore this pull-up can't be too weak.

*** BEWARE: CLOSE position 4 of DIP switch for proper startup of Nina ***

NINA_SW12 pulled up selects normal boot.
Using large R because same pin becomes LED_G output
after startup (LED not implemented) -- which gets driven
anyway by NINA hence current cons.
Option to eliminiate this extra power consumption by opening switch after startup.

*** BEWARE: CLOSE position 5 of DIP switch of STM8 not programmed / not placed ***
Open once STM8 is programmed, to optimize system deep sleep current

H1 MOUNT-HOLE-2.8
H2 MOUNT-HOLE-2.8
H3 MOUNT-HOLE-2.8
H4 MOUNT-HOLE-2.8

Selection/configuration switches

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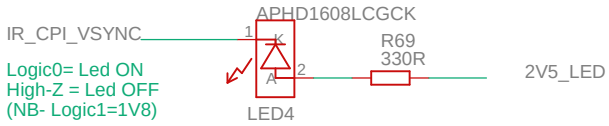
Status LED for IR Sensor Bring-up/Debug
Switch off 2V5_LED (cf DIP Switch) to save power
when not required

[Also See Note on LEDS on sheet 5]



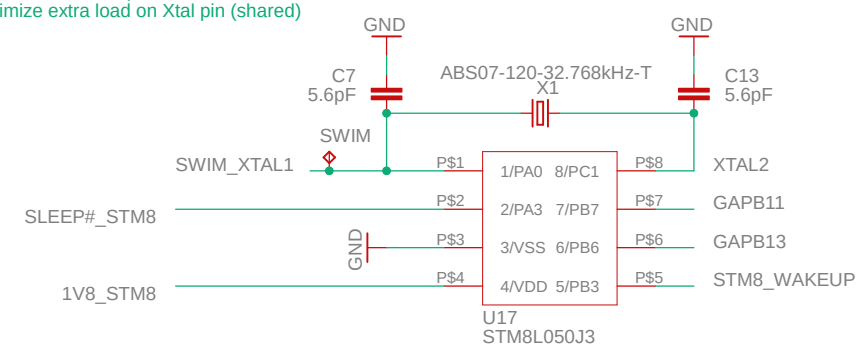
Logic0= Led ON
High-Z = Led OFF
(NB- Logic1=1V8)

Biased for I~2mA

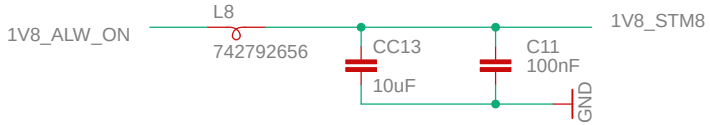
[OPTIONAL -- this provides System Watchdog + RTC functionality + helps getting to ultra-low system sleep power consumption
** Assembly Option **]

Xtal can be avoided if no RTC required, wake-up from external source only
or
if very approximate RTC (hence wake-up) period is acceptable.

Place caps cand XTAL closest to STM8 pins.
Short SWIM wires to minimize extra load on Xtal pin (shared)



Filter supply to STM8 + local bulk cap
to avoid 1V8_STM8 dropping and STM8 rebooting
(brownout reset) when system power is switched
back on at exit of system sleep



Control of system sleep mode / WatchDog

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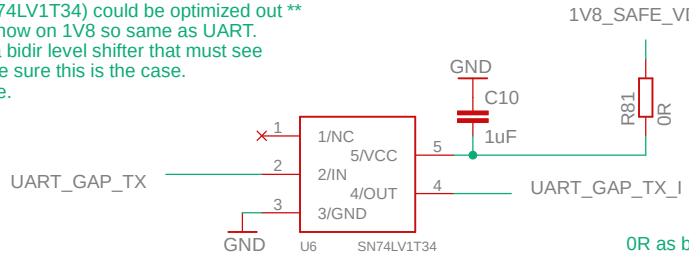
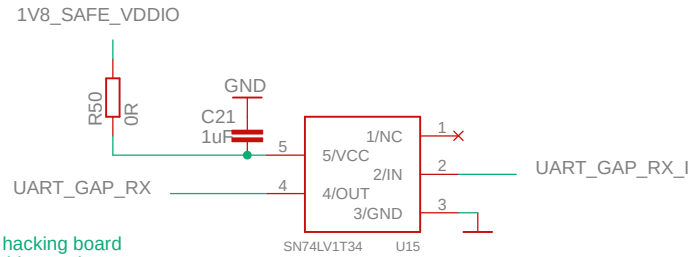
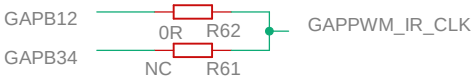
** These 2 buffer/level shifters (SN74LV1T34) could be optimized out **
Was useful when Nina was on 3V, now on 1V8 so same as UART.
However on GAPMOd1.2 there is a bidir level shifter that must see
high-Z on its outputs. Here we make sure this is the case.
Keep for now, to be on the safe side.



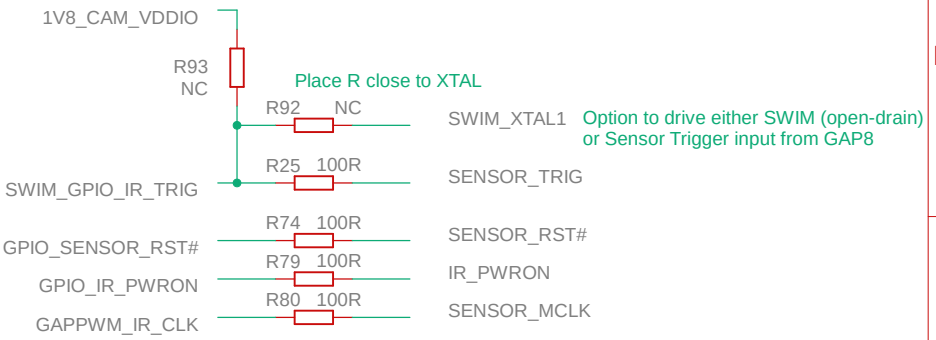


0R as back-up to allow hacking board
in case of issues using this supply

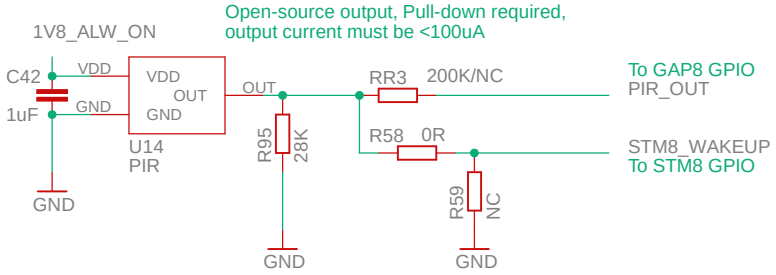
Both I/OSs are Timer/PWM capable



Padframe bug on B34 in CTu1.0/1.1 ==> don't use B34 as PWM,
instead use GAPB12 as PWM_IR_CLK
(however keep option to use B34 for when bug fixed
as it allows to use IR snesor w/o 1V8 on)



PIR usable to Wake-up GAP8 or STM8



If RR3 implemented then PIR can also wake up GAP8
however in system deep sleep with GAP8 unpowered,
will draw 9uA from PIR (if present)

Level Shifter & Misc.

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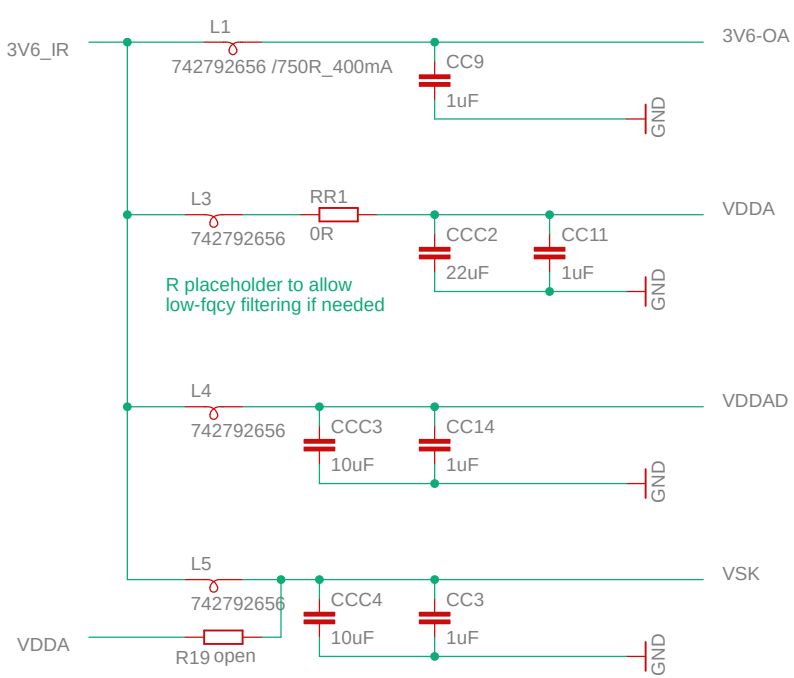

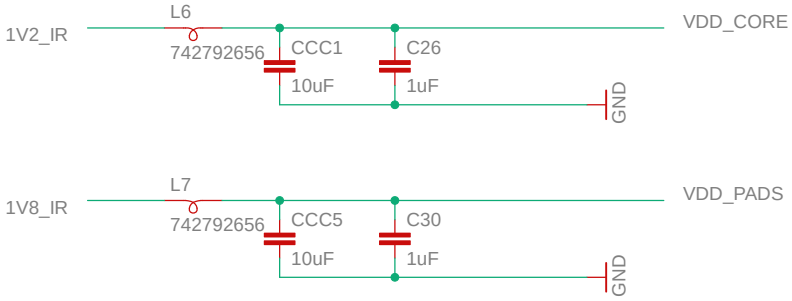

Caps named Cx are 0402 (imp.) dimensions, X5R or X7R dielectric
CCx are 0603
CCCx are 0805
CCCCx are 1206
Ceramic caps effective capacitance decreases vs. nom as DC bias increase
Smaller volume caps are more sensitive to this effect than larger voluame caps.
Cap sizes here were selected to mitigate this effect.

IR Sensor (1/3)
Dediated power supply generation and filtering

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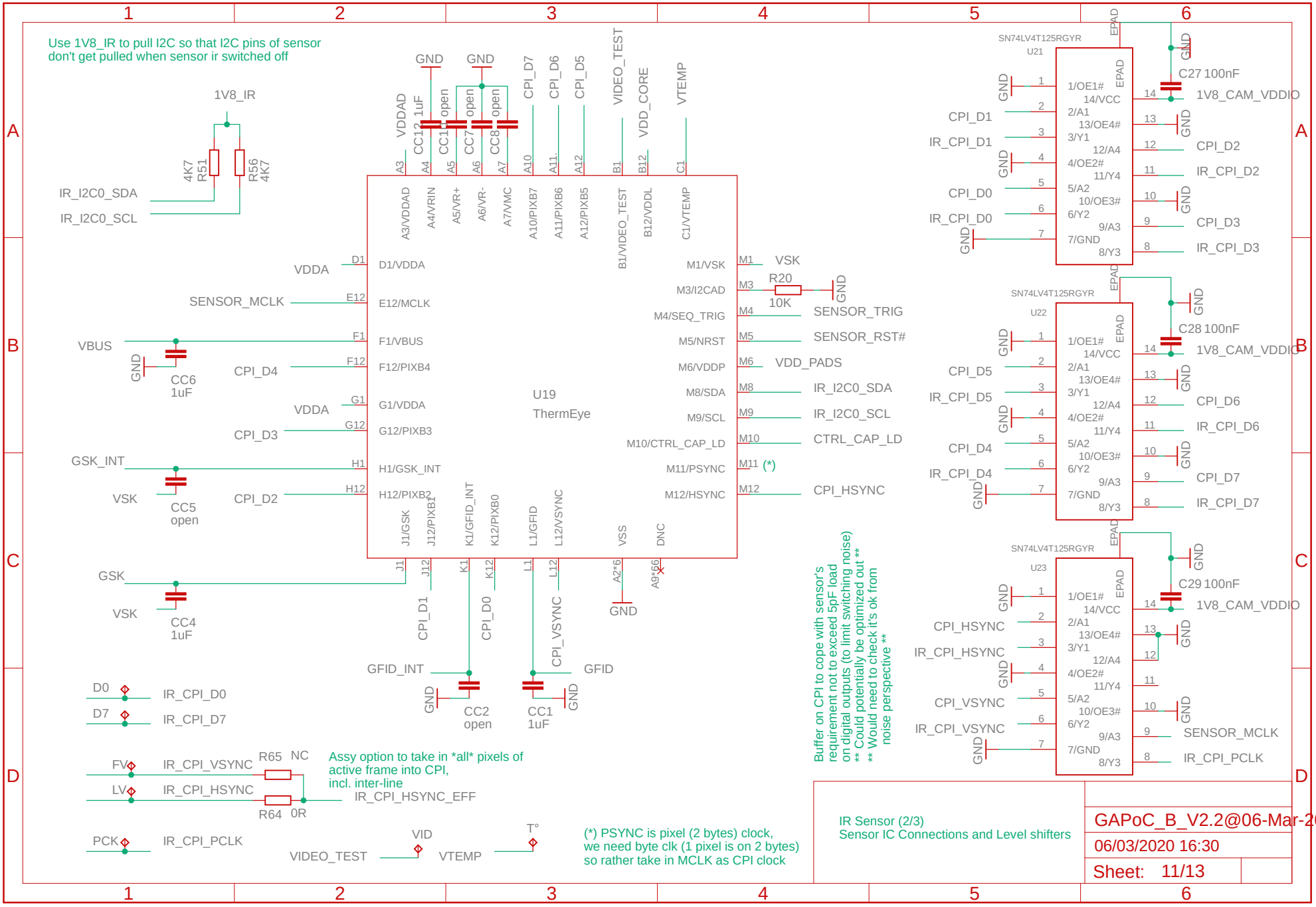
Use 1V8_IR to pull I2C so that I2C pins of sensor don't get pulled when sensor ir switched off
1V8_IR
4K7 R51
R56 4K7
IR_I2C0_SDA
IR_I2C0_SCL
VDDAD
CC12 1uF
CC11 open
CC7 open
CC8 open
GND
GND
CPI_D7
CPI_D6
CPI_D5
VIDEO_TEST
VDD_CORE
VTEMP
U19
ThermEye
D1/VDDA
E12/MCLK
F1/VBUS
F12/PIXB4
G1/VDDA
G12/PIXB3
H1/GSK_INT
H12/PIXB2
J1/GSK
J12/PIXB1
K1/GFID_INT
K12/PIXB0
L1/GFID
L12/VSYNC
VSS
DNC
M1/VSK
M3/I2CAD
M4/SEQ_TRIG
M5/NRST
M6/VDDP
M8/SDA
M9/SCL
M10/CTRL_CAP_LD
M11/PSYNC
M12/HSYNC
VDDA
SENSOR_MCLK
VBUS
CPI_D4
VDDA
CPI_D3
GSK_INT
VSK
CPI_D2
GSK
VSK
VSK
R20
10K
SENSOR_TRIG
SENSOR_RST#
VDD_PADS
IR_I2C0_SDA
IR_I2C0_SCL
CTRL_CAP_LD
(*)
CPI_HSYNC
CC6 1uF
CC5 open
CC4 1uF
CC2 open
CC1 1uF
GFID_INT
GFID
CPI_D1
CPI_D0
CPI_VSYNC
D0
D7
IR_CPI_D0
IR_CPI_D7
FV
LV
IR_CPI_VSYNC
IR_CPI_HSYNC
R65 NC
R64 0R
IR_CPI_HSYNC_EFF
Assy option to take in *all* pixels of active frame into CPI, incl. inter-line
PCK
IR_CPI_PCLK
VIDEO_TEST
VID
VTEMP
T°
(*) PSYNC is pixel (2 bytes) clock, we need byte clk (1 pixel is on 2 bytes) so rather take in MCLK as CPI clock
Buffer on CPI to cope with sensor's requirement not to exceed 5pF load on digital outputs (to limit switching noise)
** Could potentially be optimized out **
** Would need to check it's ok from noise perspective **
SN74LV4T125RGYR
U21
U22
U23
1/OE1#
2/A1
3/Y1
4/OE2#
5/A2
6/Y2
7/GND
8/Y3
9/A3
10/OE3#
11/Y4
12/A4
13/OE4#
14/VCC
EPAD
C27 100nF
C28 100nF
C29 100nF
1V8_CAM_VDDIO
CPI_D1
IR_CPI_D1
CPI_D0
IR_CPI_D0
CPI_D2
IR_CPI_D2
CPI_D3
IR_CPI_D3
CPI_D5
IR_CPI_D5
CPI_D4
IR_CPI_D4
CPI_D6
IR_CPI_D6
CPI_D7
IR_CPI_D7
CPI_HSYNC
IR_CPI_HSYNC
CPI_VSYNC
IR_CPI_VSYNC
SENSOR_MCLK
IR_CPI_PCLK
IR Sensor (2/3)
Sensor IC Connections and Level shifters
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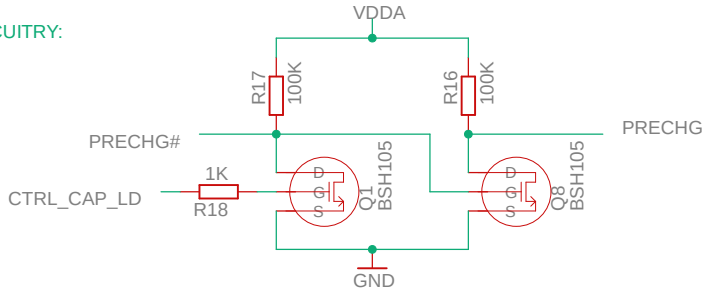
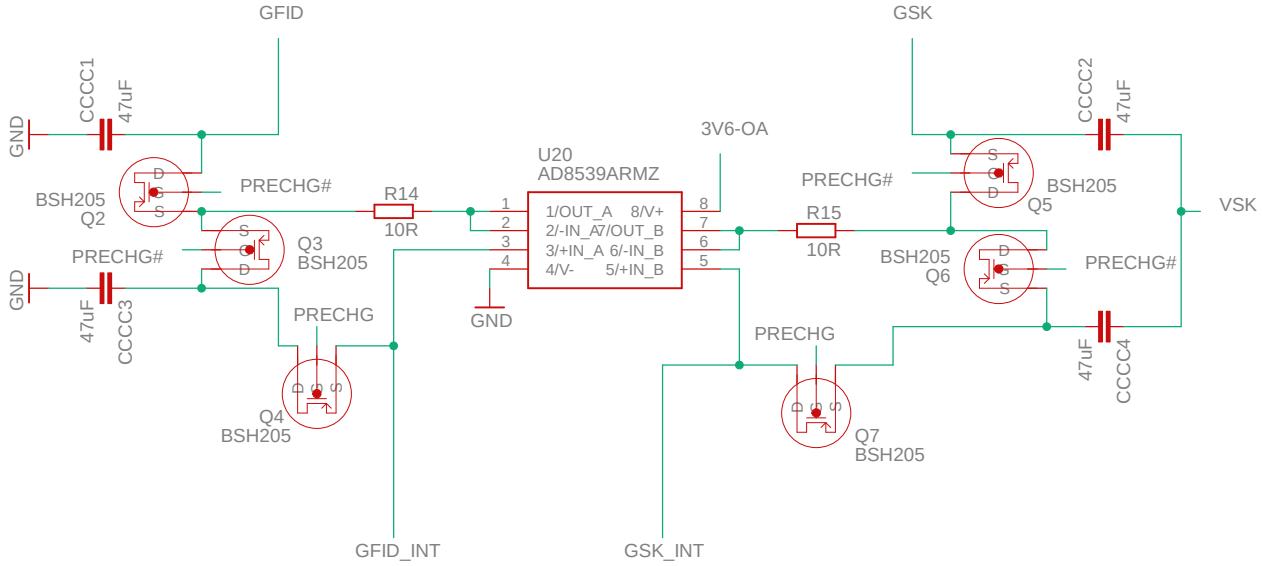
GENERATION OF PRECHARGE SIGNALS FOR BOOST CIRCUITRY:



GENERATION OF GFID AND GSK USING "TIME BOOST" :



IR Sensor (3/3)
Biasing with time boost

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