Thermal-IR GAPPoc
(GAPPoc B 2.x)

DOCUMENTATION

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CONTENTS

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0. Quick Start guide for the impatient

This is a summary of key steps to start the Thermal-IR GAPPoc. It is highly recommended to go through the full document to understand the system.

1) Set DIP switch in a suitable configuration – see section 4. Typically:
- Position 1: open to minimize power / close to Enable 2.5V supply to eFuse+LEDs
- Position 2: open (Assign UART to Nina BLE)
- Position 3: open to minimize power / close to Enable Status LEDs (with pos.1 closed too)
- Position 4: close (normal Nina BLE boot)
- Position 5: close (ensure sleep mode is off at start-up)
- Position 6: open to minimize power / close to Enable User LED (with pos.1 closed too)

2) Connect battery:
> Insert a **3.6V lithium** battery (for example, SAFT 14500 or equivalent) in the on-board AA holder. Never exceed 3.7V across terminals of the on-board single AA battery holder.
> **Alternatively**, it is also possible to connect an external battery holder through the JST connector; however :
- on GAPOC B 2.2: not recommended, or take care not to exceed 3.6V (beware that fully charged NiMh/Alkaline batteries provide higher voltage than their nominal value).
- with GAPOC B 2.3/2.4: voltage on JST connector may reach 5.5V.
See section 6 dedicated to power sources, p12.

- If you want to test a pre-flashed board (programmed to boot from external Flash)
3a) Switch power on (general ON/OFF switch)
4a) Press reset button (marked RST# on board) on GAPPoc B 2.2

- If you want to program the GAP8 chip :
3b) Connect your JTAG probe
4b) Switch power on (general ON/OFF switch)
5b) Program GAP8 from your PC through JTAG

Like any uncased electronic equipment, **this board is sensitive to Electro-Static Discharges (ESD)**. Make sure you are not electro-statically charged before handling the device (wear an anti-ESD writsband or touch first some object connected to earth).

1. Introduction

GAPPoc Concept
GAPPoc is an acronym for GAP8-centric Proof Of Concept. GAPPoc comes in different flavors for different classes of applications. The objective of GAPPoc boards is to build credible demonstrators, representative of a final application in terms of features, performance, power consumption and form

factor (as far as possible, as board size and shape cannot be fully optimized independently from final product constraints). Design choices are intended to shorten time to functional POC and to ease redesign of GAPPoc to go from target application X to target application Y.

Any GAPPoc is architecture around a GAPmod *[Ref.1]* core module (which itself essentially embeds a GAP8 chip, external memory (Flash + RAM), a 32.768KHz crystal and power management for core power and crystal oscillator supplies), augmented with functionalities in line with the target applications (especially sensors and radio), on-board generation of all power supplies, plus various expansion/monitoring connectors.

Thermal-IR GAPPoc

This variant of GAPPoc (board ref. "GAPPoc B 2.x") enables the demonstration of applications that would analyze/interpret scenes using low-resolution and low-cost Thermal Infra-Red sensors and provide results in a compact (hence low bandwidth) form over a radio link – specifically, Bluetooth Low Energy here.
A typical use case is people counting in rooms with a Thermal-IR GAPPoc installed on the ceiling.

2. High-level architecture

The general architecture of the Thermal-IR GAPPoc is outlined in Figure 1.

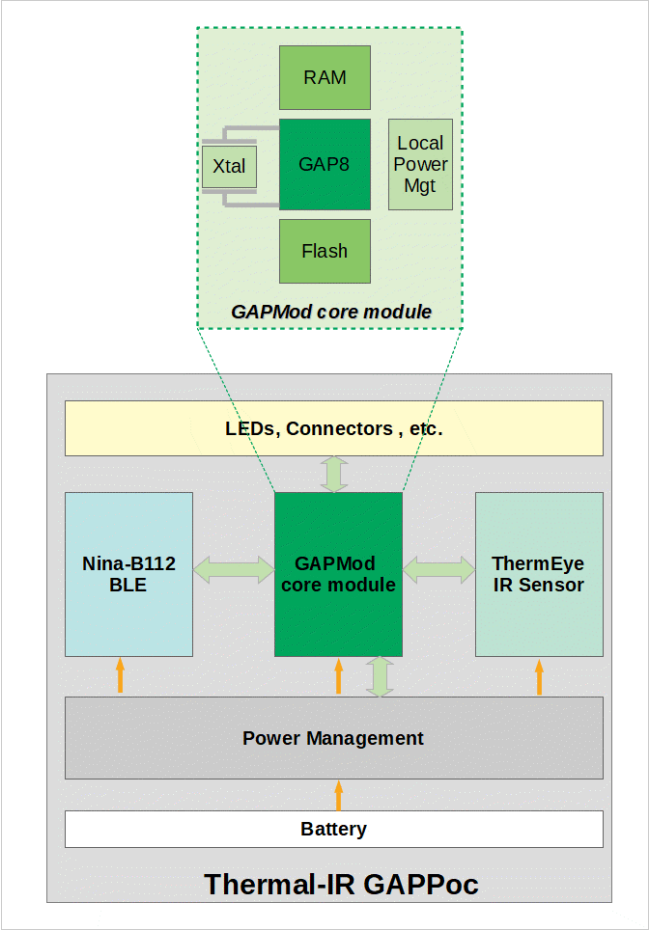


Fig. 1 – GAPPoc B 2.x Architecture Outline

3. Board Anatomy

Thermal-IR GAPPoc (GAPPoc B 2.x) includes :

Main components (with reference to Fig. 2.a) :
> (1) Either GAPMod1.2 core module with 64Kbit RAM and 512Kbit Flash on HyperBus,
or GAPMod2.x core module with 64Kbit RAM and 128Kbit Flash on Quad-SPI Bus,
> (2) Lynred's ThermEye120 Thermal Infra-Red sensor,
> (3) uBlox NINA-B102 Bluetooth Low Energy (BLE) module with integrated antenna and pre-Flashed firmware to support GATT profiles through AT commands and a Serial Port Service ("wireless UART").
> (4) Slot for a through-hole PIR
> (5.a, 5.b) AA cylindrical battery holder, plus JST battery connector for separate holder of 3 AA/AAA NiMh batteries. Do not exceed 3.6V nominal voltage at battery connector terminal.
> (6.a and 6.b) 2.54mm pitch expansion female connectors, dual-entry
> (7) 10-pin, 1.27mm pitch male JTAG connector.

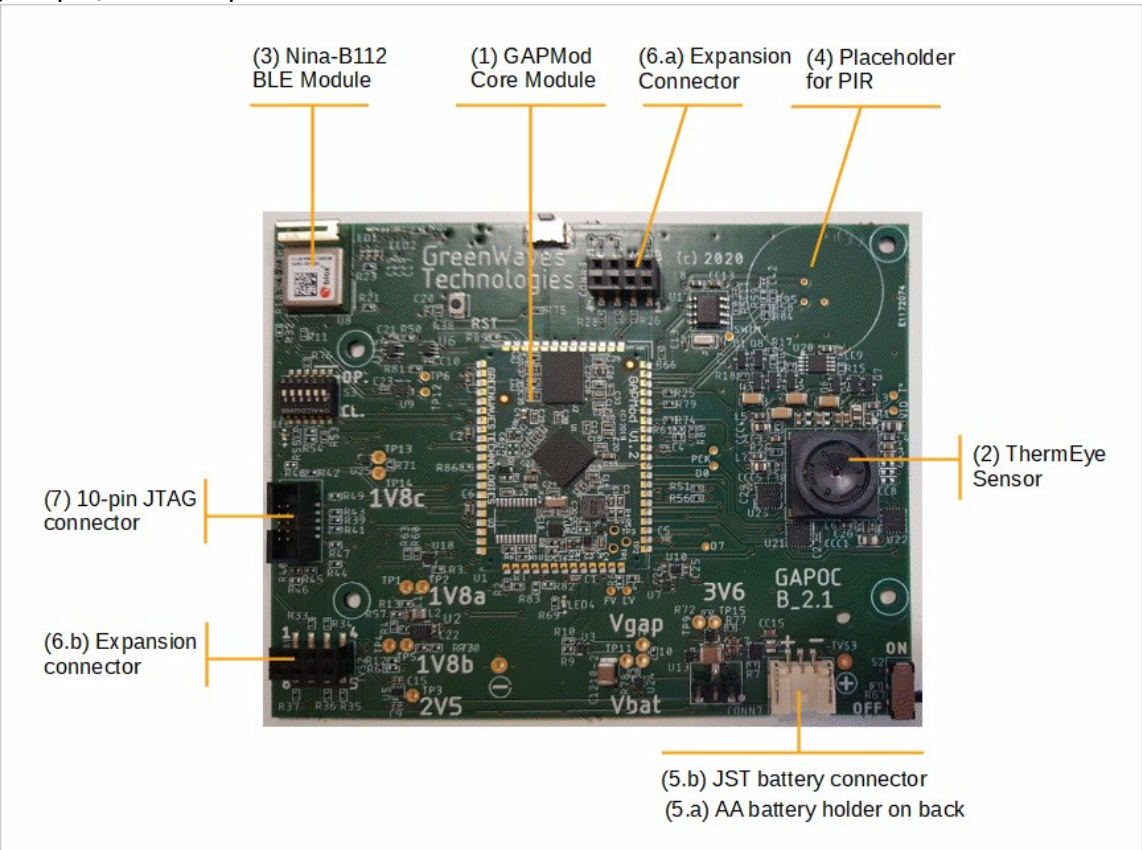


Fig. 2.a – Anatomy of GAPPoc B 2.x : Main components

Control and status (with reference to Fig. 2.b) :
> (8) General ON/OFF switch
> (9) Mini-DIP switch LED to set some static configurations (see also section 4 below)
> (10) Hardware reset push-button

> (11) Generic push-button whose status can be monitored by s/w through a GPIO
> (12) (LED1+LED2) BLE status LEDs – One dual LED + One single LED
> (13) (LED4) Vsync status LED (LED4), toggles when IR Sensor sends data frames to GAP8
> (14) (LED3) Generic user LED, software controllable thorugh a GPIO
See also sections 5 below for information on LED and push-button control

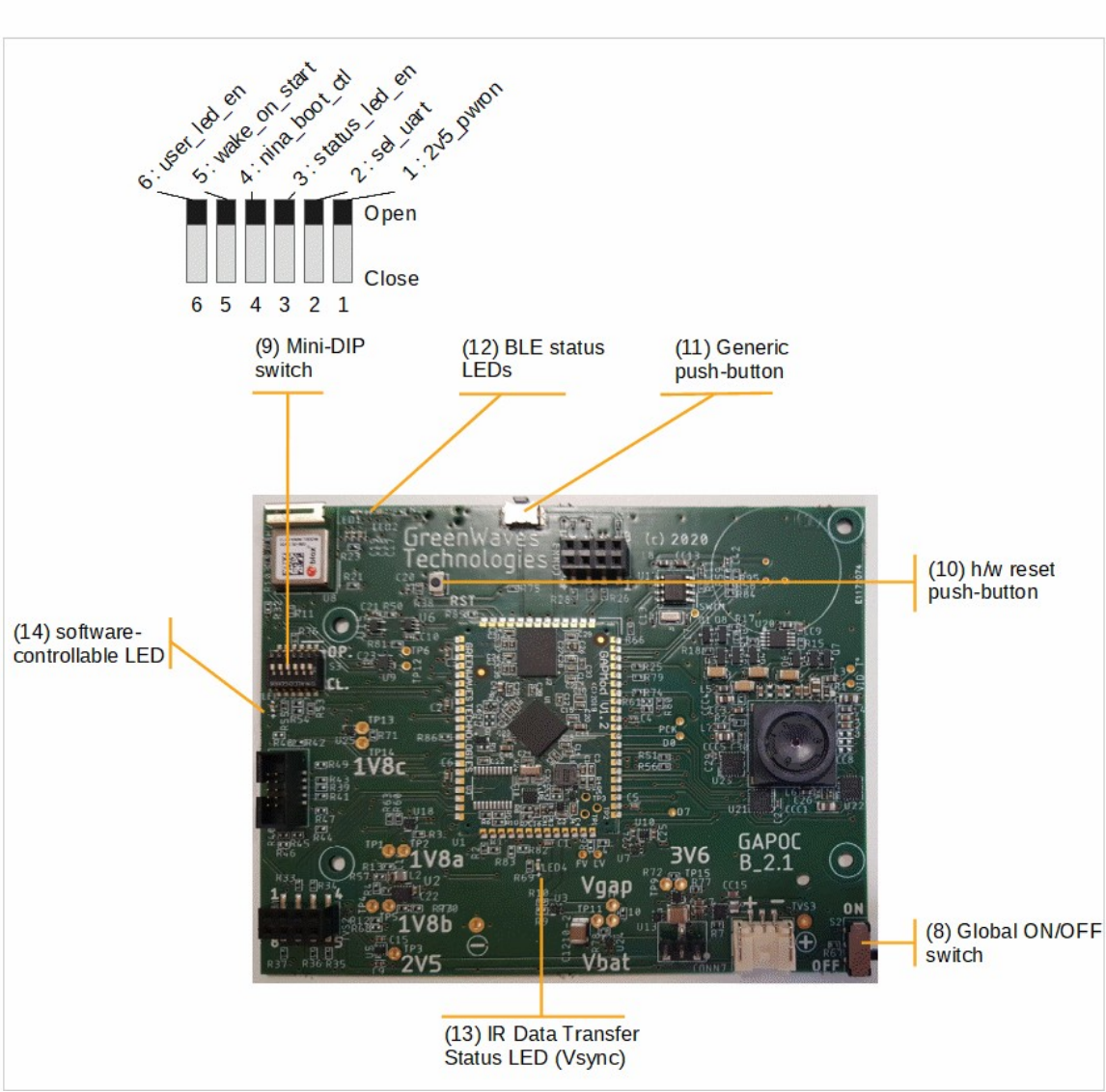


Fig. 2.b – Anatomy of GAPPoc B 2.x : Control and Status

Test Points / Injection points (with reference to Fig. 2.c) :

Note:

When 2 testpoints are mentioned for a given power supply, **those 2 tespoints are separated by a 0.5ohm current sensing resistor,** for measuring current consumption. The current flowing between the test points is therefore **I=2xV** where V is the voltage difference between these two test points.

At 0.5ohm, the sense resistance is deliberately small to avoid severe supply voltage fluctuations when there are significant instantaneous current changes. To completely eliminate the influence of this resistor, it is always possible to short the 2 test points externally. Conversely, to measure very small current, the 0.5 ohm resistor may not be appropriate; in such case R should be removed and replaced by a larger value or perhaps a suitable equipment (ammeter or other).

[See also Power Management scheme description in section 6]

> (15) Test Points **TP10-TP8**: on 1.8V supply going, if enabled, to Nina BLE

> (16) Test Points **TP1-TP2**: on 1V8_ALW_ON ("always-on" output of 1.8V DC-DC converter) – feeding STM8 and, if enabled, 1V8_MEM going to external memories and SPIM_VDDIO supply of GAP8.

> (17) Test Points **TP4-TP5**: on 1V8_GATED ("switchable" output of 1.8V DC-DC converter) – root voltage source for: 1.8V to SAFE_VDDIO supply of GAP8, 1.8V to CAM_VDDIO supply of GAP8, 1.8V supply for ThermEye module I/Os, plus LDO generating 1.2V for ThermEye digital core.

> (18) Test point **TP3** (single test point): on 2.5V, used as Fuse programming voltage (VQPS) and power supply of on-board LEDs (if enabled)

> (19) Test points **TP10-TP7** : on VBAT going to internal DC-DC converter of GAP8 (which feeds GAP8's digital core)

(note it is also possible to probe power consumption of GAP8 digital core after DC-DC conversion on **GAPMod)**

> (20) Test points **TP10-TP11** : on VBAT going to 1.8V DC-DC converter, represents the "root" currrent under VBAT voltage required by the 1.8V DC-DC converter to produce the sum of currents (under 1.8V) measured through TP1-TP2 (1V8_ALW_ON) plus TP4-TP5 (1V8_GATED)

> (21) Test points **TP9-TP15** : on 3.6V going to ThermEye thermal IR sensor (analog core)

> (22) Test points **TP6-TP12** / **UART_FROM_EXT-UART_TO_EXT**: *if mini-DIP switch position #2 is closed*, these TP connect to the UART input Rx (for TP12/UART_FROM_EXT) and output Tx (for TP6/UART_TO_EXT) of GAP8. *Beware, there are 1.8V level signals; do not connect directly to higher voltage signals (use level shifters or current limiting series resistors to connect to e.g. 2.5V or 3V levels).*

> (22) Test points **FV** and **LV**: FV is the Frame Valid (Vsync) signal from the ThermEye sensor, LV is Line Valid (Hsync)

> (23) Test points **PCK** and **D0**: PCK is the pixel clock fed to GAP8 (*note* – is obtained from the master clock of ThermEye rather than its pixel sync output, due to ThermEye peculiarities), D0 is the LSB of the pixel data bus.

> (24) STM8 programming interface (**SWIM**) : this point provides access to the SWIM I/O of STM8, usable for programming/debugging it.

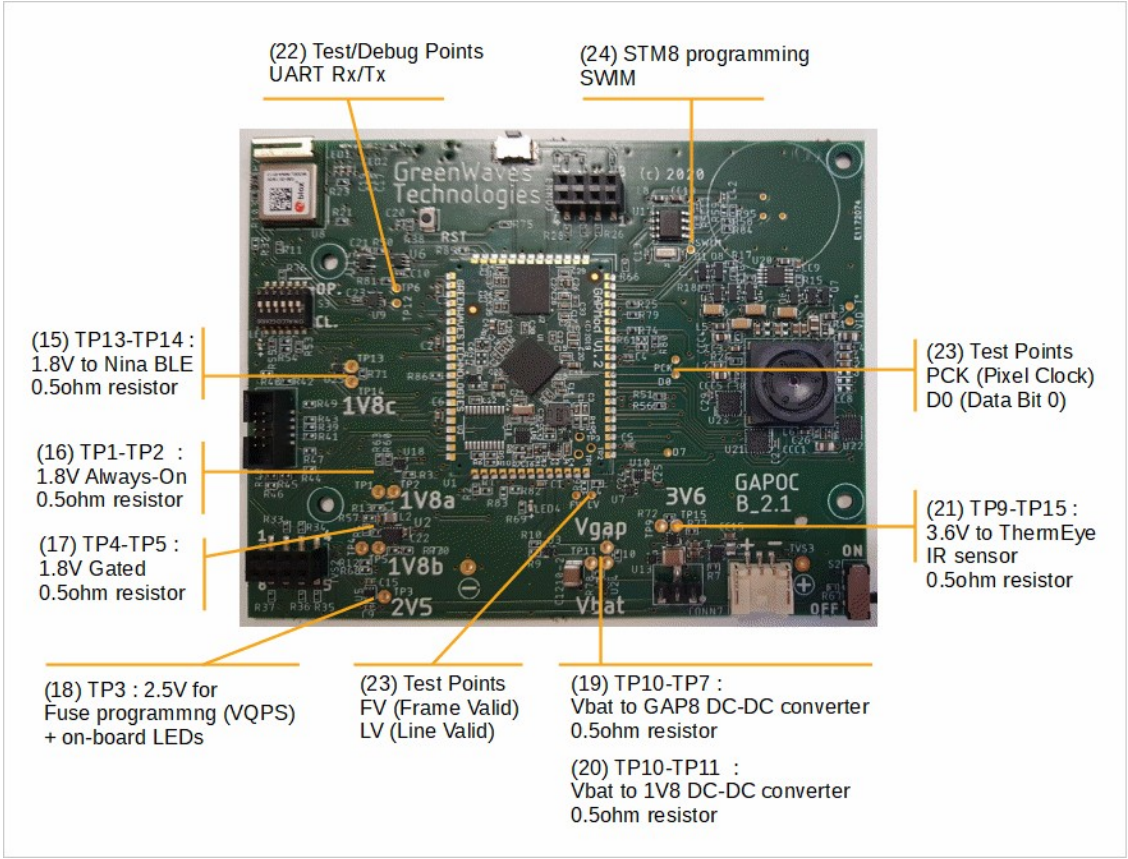


Fig. 2.c – Anatomy of GAPPoc B 2.x : Test Points

Programming of GAPPoc boards is possible using an **OpenOCD-compatible JTAG probe.**
An example is Olimex's ARM-USB-OCH-H model, coupled with an adapter JTAG-20-pin/2.54mm pitch to 10-pin/1.27mm pitch (ARM-JTAG-20-10) *[Ref.5]* as show in Figure 3.
J-Link probes from Segger have also been tested succesfully.

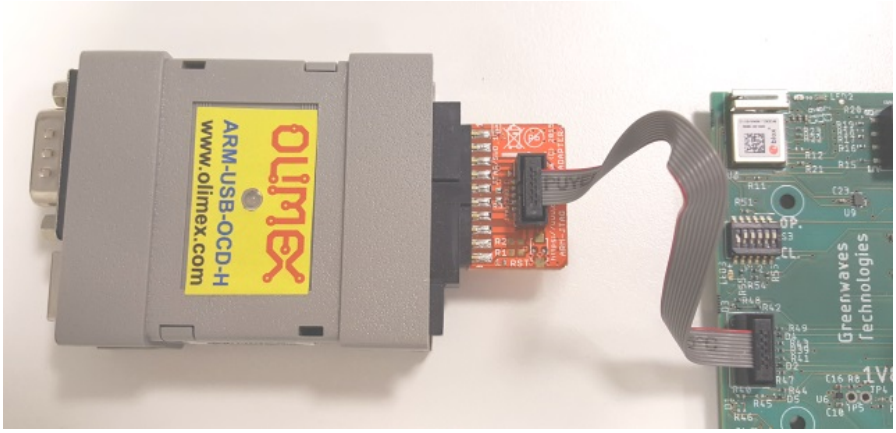


***Fig. 3** – OLIMEX probe with JTAG-20-10 adapter*

4. Mechanical Switches and Jumpers

Global ON/OFF switch (S2):

> Item (8) in Fig. 2.b.

S2 is a slider switch that completely powers on/off the full board (with the exception of the boost converter from Vbat to 3.6V – whose quiescent current is very low, at 1 uA typ.)

Make sure S2 is OFF when board is not in use to maximize battery lifetime (unless GAP8 firmware is already optimized for ultra-low power sleep mode)

Manual Reset button (S1):

> Item (10) in Fig. 2.b.

When S2 is pushed, the hardware reset input of GAP8 (NRESET) is pulled low (reset asserted).

Miniature DIP Switch (S3):

> Item (9) in Fig. 2.b.

This mini-DIP switch provides 6 individual switches which can be used to change some board configurations.

Their functions are as follows (see also Fig. 2.b):

*[Numbering of switch positions **starts from the side with the OP.(open)/CL.(close) legend marking** on PCB]*

> Pos. #1: 2V5_PWR_ON

Open : 2.5V power supply is OFF; in this case GAP8's Fuses cannot be programmed (pin VQPS is not powered) and **on-board LEDs are not powered**. This setting is useful when looking for minimum overall board consumption.

Closed: 2.5V power supply is ON. Fuses can be programmed. On-board LED are powerable, actual enabling is controlled through additional configuration switches, see below.

> Pos. #2: SEL_UART (*)

Open : GAP8's UART is routed to NINA BLE module.

Closed: GAP8's UART is routed to TP6 (TX from GAP) and TP12 (RX to GAP).

> Pos. #3: STATUS_LED_EN (*)

Open : 2.5V to LED1+LED2 (BLE status) and LED4 (Vsync status) is gated off, LEDs are not active

Closed : LED1+LED2(BLE status) and LED4 (Vsync status) are enabled; they reflect status of BLE connection and Vsync activity.

> Pos. #4: NINA_BOOT_CTL (*)

Open : pins NINA_SW1 and NINA_SW2 of the NINA BLE module are not pulled.

Closed : pins NINA_SW1 and NINA_SW2 of the NINA BLE module are pulled high.

Refer to Nina-B112 module datasheet for details on the role of those pins.

This switch must be closed for normal start-up of the Nina module. It can then be closed to minimize static power consumption, see section on Nina BLE module.

> Pos. #5: WAKE_ON_START

Open : signal SLEEP# (system-wide sleep enable signal) is not pulled at start-up. This setting should be used only if the (optional) on-board STM8 has been programmed with appropriate firmware and deep optimization of sleep current is required.
Closed : signal SLEEP# is pulled down at start-up. This setting makes sure system will start up properly independently from presence/programming of on-board STM8. It will add about 9uA additional consumption in system deep sleep if kept closed.

> Pos. #6: USER_LED_EN (*)
Open : LED3 ("user LED") is disconnected from GAP8 pin A3.
Closed : LED3 is connected with GAP8 pin A3 and can be freely controlled by the user by configuring pin A3 as GPIO. Drive to Logic 0 to turn LED on and to high-Z (or set as input) to turn LED off. See also former paragraph about LED3.
Note the signal from pin A3 is made available on pin 2 of expansion connector CONN3 – so in many cases usage of this connector pin will have to be exclusive with usage of LED3.

(*) Also refer to Section xx on Resource Sharing

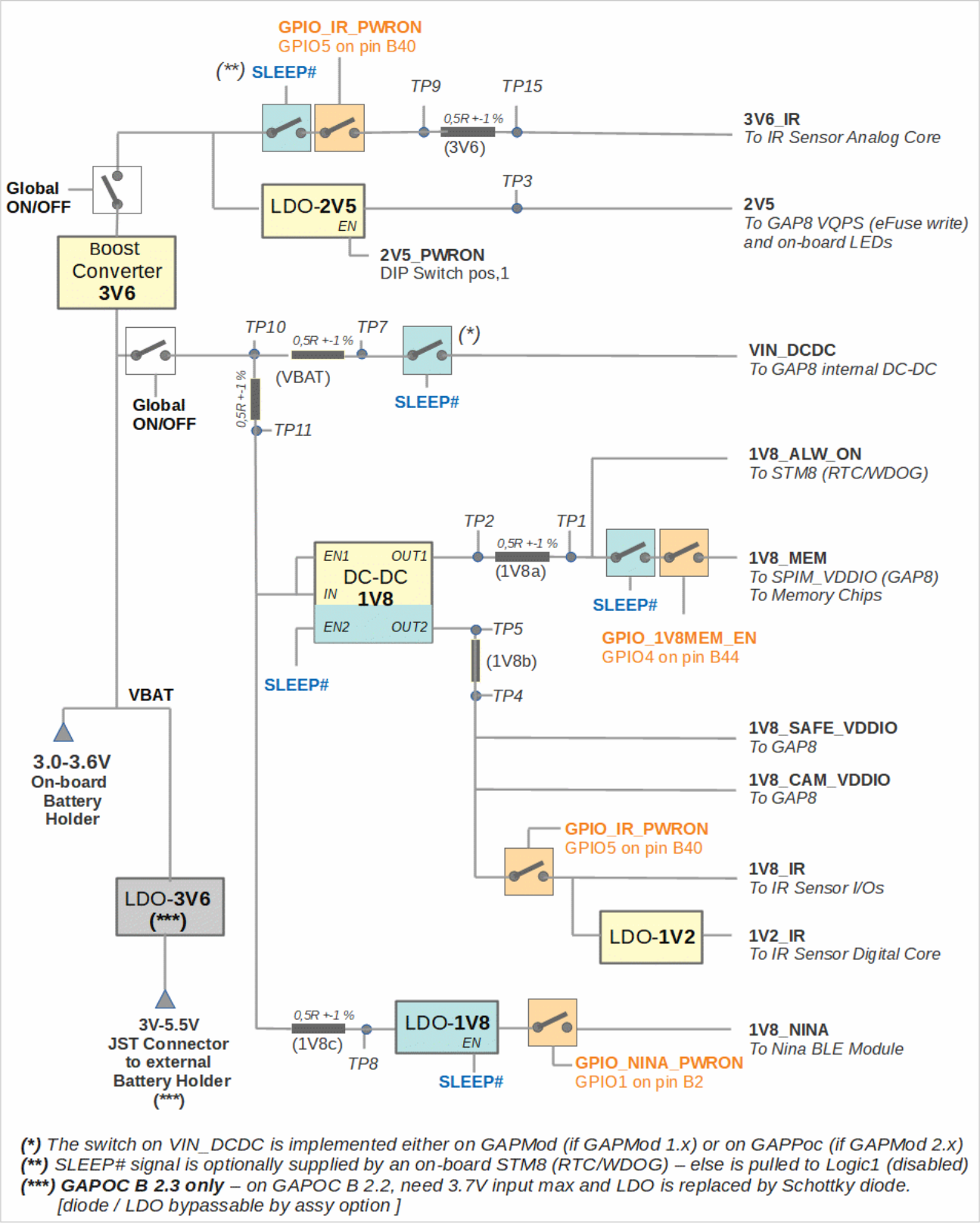
5. Monitoring LEDs

"User LED" LED3:
> Item (14) in Fig. 2.b.
LED3 is available to the application running on GAP8. **To use it, both positions #1 (2V5_PWR_ON) and #6 (USER_LED_EN) on the miniature DIP switch S3 (see above) must be closed**. Then :
- drive a **Logic0** on pin A3 configured as GPIO to turn LED **ON** ,
- set pin A3 into **high impedance** (or set as input) to turn LED **OFF**.
Note: driving a Logic1 does not turn LED completely off, set to High-Z instead.
(so beware: the LED expects an open-drain, **"active low" behavior**)
The LED consumes in the 2mA range when ON. When OFF (A3 high-Z) it might still consume a few uA. When power consumption needs to be fully optimized, cut power to the LED by opening position #6 of the mini-DIP switch (USER_LED_EN).

BLE Status LEDs (LED1+LED2) :
> Item (12) in Fig. 2.b.
LED1 is a single LED that connects to the "BLUE" output of NINA (see Nina-B112 datasheet *[Ref.3]*) – although it's not blue on the board.
LED2 is a dual-color Red + Greenish-Yellow LED; the Greenish-Yellow component is ON as soon as 2.5V power supply is present (enabled/disabled by DIP switch), the Red Component connects to the RED output of NINA.
As a result :
- LED1 will be ON when the Nina BLE module is connecting (using SPS proprietary serial mode profile) and will flash on data activity.
- LED2 will be Greenish-Yellow in Idle Data Mode and when Connected, Orange in Idle command Mode and when connecting.

Infra-Red Data Transfer (Vsync) Monitoring LEDs (LED4) :
> Item (13) in Fig. 2.b.
when this LED is enabled (thorugh miniature DIP switch positions 1 and 3), it will be ON by default and flash OFF during transfer of data from ThermEye sensor to GAP8 (specifically, it will be turned off by Vsync being high).

6. Generation, control and monitoring of on-board power supplies



***(*)** The switch on VIN_DCDC is implemented either on GAPMod (if GAPMod 1.x) or on GAPPoc (if GAPMod 2.x)*
***(**)** SLEEP# signal is optionally supplied by an on-board STM8 (RTC/WDOG) – else is pulled to Logic1 (disabled)*
***(***) GAPOC B 2.3 only** – on GAPOC B 2.2, need 3.7V input max and LDO is replaced by Schottky diode.*
[diode / LDO bypassable by assy option]

Fig. 4 – On-board power supply generation and control (notional) – TO UPDATE

– Battery / Main Power Source –

Power can be supplied to the board by different means :

1) Recommended: on-board battery holder (3.6V nom.):
the on-board battery holder is intended to house a **single 3.6V lithium battery, AA size** (lower voltages down to 3V minimum are also acceptable). Never exceed 3.7V.

Or

2) JST connector to external battery pack (3V-4V):
Please check marking close to the bottom right corner of the board to identify version
> with version 2.2 of GAPPoc B:
it is not recommended to use the alternative JST connector and an external battery holder unless you take specific precautions. Battery voltage must be between 3V and 3.6V ; exceeding 3.6V may damage some components. Pay attention to the fact that voltage across terminals of fully charged batteries may be higher than nominal voltage (for example, even though 3x NiMh batteries would be expected to provide 3x1.2V =3.6V nominal, each cell can actually start from 1.3V-1.4V at full charge).
> with version 2.3/2.4 of GAPPoc B:
it is possible to connect through this JST connector a battery holder containing **three (3) or four (4) AA/AAA NiMh rechargeable batteries** (1.2V each, nom.) in series – not exceeding 5.5V total. **Do NOT use primary alkaline batteries (1.5V each nom.)** as the total voltage when fully charged can exceed the 5.5V limit supported by GAPPoc B 2.3/2.4 on this input.

Or:

3) external power supply :
for development, an external power supply can be connected to battery holder terminals, delivering a voltage between 3V and 3.6V.

In all cases the power source should be able to deliver up to 300mW at board input (for example 80mA under 3.6V or 100mA under 3V, etc.) – this is for short periods of time, average power will be orders of magnitude lower.

Do not keep a battery in the on-board holder while off-board batteries (through JST connector) are being used – and vice-versa (mutually exclusive usage).

Power off the board power (using global ON/OFF slider switch) when inserting/removing batteries or JST connector.

Note:
If you are performing power measurements, you will get better results by providing power through

the on-board single AA battery holder. Power obtained through the JST connector for external batteries goes through a diode (v2.2) or an LDO (v2.3/2.4) which introduces some power loss.

– Software-controllable Power Switches –

The following GPIOs can be used to selectively switch off power supplies on the board.
They are highlighted in orange on Figure 4 (Power Supply Generation and Control).

> GPIOA4 on GAP8 pin **B44** = **GPIO_1V8MEM_EN**,
controls **1.8V to External Memories + SPIM_VDDIO**
Notes:
- if 1.8V is switched off, all code after this operation must be fetched from internal memory only, until 1.8V is enabled back.
- driving the 1.8V enable signal low (1.8V off) draws about 1.8uA (except if the SLEEP# signal is asserted), due to a weak pull-up to SAFE_VDD_IO (1.8V) on this signal. On the other hand, an alternative option to cut power drawn from the 1.8V supply is to put the external memory in deep power-down. These factors should be taken into consideration to decide the best option.
- switching off this 1.8V supply also means the full SPIM_VDDIO portion of GAP8's I/O ring is switched off, which not only includes the memory I/Os but also a few others, including UART (refer to GAP8 datasheet *[Ref.1]*).

> GPIOA5 on GAP8 pin **B40** = **GPIO_IR_PWRON**,
controls **Power Supplies to ThemEye IR Sensor :**
- if this GPIO is low, all power supplies to the ThermEye IR sensor are switchted off: 3.6V to analog core, 1.8V to ThermEye I/Os and 1.2V to digital core

> GPIOA1 on GAP8 pin **B2** = **GPIO_NINA_PWRON**,
controls **Power Supply to Nina BLE Module :**
- if this GPIO is low, the full Nina BLE module is powered off

– Statically Configurable Power Switches –

> Global Power ON/OFF
Mechanical slider switch to cut off board power, see Section 4.

> 2V5_PWRON:
Mini-DIP switch to enable 2.5V power supply to VQPS pin (for eFuse programming) and to on-board LEDs. See Section 4.

– System-wide Power Off (System Deep Sleep) –

> SLEEP#

An on-board, low-cost 8-bit MCU (STM8L050J3) can be used, with appropriate firmware, to act as system-wide WatchDog and RTC and to generate a SLEEP# signal able to cut power to almost all boards components.
When this signal is low (asserted), only an always-on 1.8V supply is provided to:
- the STM8 itself (which would typically be put in ultra-low power halt mode with RTC active),
- the VDD pin of the placeholder for optional PIR,
Also (in current board version) the 3.6V boost converter stays powered from VBAT (TPS610995, with IDDq~1uA)

– Test Points / Power Supply Monitoring –

Several test points are provided to monitor supply voltages or supply currents.
Refer to Section 3 (Board Anatomy) for location and role of each test point.
To monitor current, Test Points are arranged in pairs with a 0.5ohm (+-1%) sense resistor on the current path between each element of the pair. This means the current going through the sense resistor (in mA) is twice (2x the value of the voltage drop (in mV) measured across the sense resistor (I=U/R). The sense resistor is deliberately small to avoid severe supply voltage fluctuations when there are significant instantaneous current changes.
The test points are 2.54mm apart plated holes to allow usage of standard header pins and ease measurements.

7. GAP8 I/Os used for Control/Monitoring of on-board hardware

> Control of On-board Power Supplies :
- **GPIO_NINA_PWRON** (GPIO1 on GAP8 pin **B2**)
- **GPIO_IR_PWRON** (GPIO5 on GAP8 pin **B40**)
- **GPIO_1V8MEM_EN** (GPIO4 on GAP8 pin **A44**)

Refer to section 6 on power management above.

> ThermEye IR Sensor Control:
- **GPIO_SENSOR_RST#** (GPIO16 on GAP8 pin **D1**)
  This GPIO driectly drives the hardware reset input (active low) of the ThermEye IR Sensor
- **GPIO_IR_TRIG** (GPIO3 on GAP8 pin B1)
  This may be used as a hardware frame capture trigger by the ThermEye sensor. Usage is not mandatory as capture can also be triggered in software, writing to a register.
- **GAPPWM_IR_CLK** = GAP8 pin **B12** = (+assembly option to use B34 instead)
  This pin of GAP8 must be configured in PWM output mode to generate a suitable master clock for the ThermEye IR sensor (800KHz max).

> PIR Monitoring (if PIR present)

- **PIR_OUT** (GPIO2 on GAP8 pin **A2**)
  This GPI0 captures the state of the on-board PIR sensor (Logic1 if movement detected, Logic0 otherwise)

> Generic Push-button
- **GAPA13_PBUTTON** (GPIO18 on GAP8 pin **A13**)
  This GPIO captures the state of the generic on-board push-button (item 11 in Figure 2.4): Logic0 if being pushed, Logic0 otherwise.
  This GPIO is shared with position 8 of connector 3.

> User LED Control
- **GAPA3_LED3** (GPIO0 on GAP8 pin **A3**)
  This GPIO can be used to control LED3, a generic LED on the board (item 14 in Fig. 2.a); refer to section 5 ("Monitoring LEDs") above. It is active low from LED point of view and should emulate an open-drain behavior (Logic0=drive to GND, Logic1=high-Z/input).
  This GPIO is shared with position 2 of connector 3.

> NINA BLE Module Control
- **NINA_DSR/GAPA4** (GPIO0 on GAP8 pin **A4**):
If the Nina module has first been set accordingly using a suitable AT command, its DSR input pin (pin 17) can be used to enter/exit module sleep mode. Refer to the NINA-B112 datasheet *[Ref.3]* for details.
This GPIO is shared with position 4 of connector 3.
Note also that this pin and pin A3 share the same GPIO bit (GPIO0). Therefore, usage of GPIO0 on either pin A4 or pin A3 is mutually exclusive. This means it's not possible to use the User LED throgh pin A3 and at the same time use pin A4 to control Nina sleep mode.

8. GAPmod Core Module

GAPmod is a module architectured around GreenWaves Technologies' GAP8 ultra-low power Application Processor for the IoT. GAPmod packs on a small board (*ca.* 26mmx36mm) the "invariant" part of any application based on GAP8 (GAP8 chip, external Flash + RAM memory, associated decoupling caps, crystal oscillator, passives for internal DC-DC, etc.).
GAPmod is SMT assembled on GAPPoc. GAPmod gives to the motherboard (GAPPoc here) full and transparent access to the GAP8 chip it bears.
See *[Ref.1]* for a full GAPmod datasheet.

Two variants of GAPMod exist:
- GAPMod 1.x, which bears an HyperRAM+HyperFlash multi-chip module (MCM),
- GAPMod 2.x, which bears a Quad-SPI Flash chip and a Quad-SPI (PS)RAM chip

9. *ThermEye* Thermal IR Sensor Module

The ThermEye module *[Ref.2]* is a low resolution Thermal IR system which integrates an opto-electronic sensor sensitive to long wave infra-red radiation (LWIR) with a fixed lens. Two Fields of View (FOV) are available: 90° horizontal FOV (ThermEye-b90) and 120° horizontal FOV (ThermEye-b90). Currently only the ThermEye-b120 is implemented on GAPPoc boards.
The sensor is based on microbolometer technology which converts infrared radiations into an electronic signal.
Its low-resolution (80x80 pixels) helps achieve very low power consumption and reasonable cost and is sufficient for many relevant use cases. In particular, human bodies, for example, can be detected, but with no means to identify people – which steers the system clear from privacy concerns.

10. BLE Module (uBlox NINA-B112)

The Bluetooth Low Energy (BLE) module implemented on GAPPoc is a module from uBlox with integrated antenna a pre-flashed firmware supporting AT commands: NINA-B112. Refer to its datasheet for details *[Ref.3].*
GAP8 can communicate with the NINA module through the UART interface available on pins A7 (GAP UART Tx) and B6 (GAP UART Rx). Note DIP switch #2 must be open to use Nina's BLE interface, refer to Section 4.
Power supply of NINA can be completely cut off, see section on power management further up this document.
IMPORTANT : To ensure proper start-up of Nina when it's powered up, position #4 of the mini-DIP switch (NINA_BOOT_CTL) should be **closed**. This switch controls the value seen on Nina's pins SWITCH1 and SWITCH2 at start-up, which in turn control the boot mode of Nina – having SWITCH1 and SWITCH2 at Logic1 means normal start-up from pre-flashed firmware. Refer to Nina-B112 datasheet for details *[Ref.3].*

11. PIR PlaceHolder

A placeholder for a PIR Sensor is provisioned on GAPPoc. The PIR is not present by default.
That PIR could be used in use cases where the application would like to take actions when some movement is detected in front of the system.
The through holes for optional PIR assembly are compatible with the footprint of Panasonic's EVKMx family of ultra-low power PIR. These integrate the full PIR detection system: pyro-electric sensor element and Fresnel lens as well as signal conditioning to produce a ready-to-use simple Logic0/Logic1 output. Static power consumption can be as low as 1, 2 or 6 uA, making the device compatible with always-on usage in a battery powered system. Achieving this level of ultra-low power consumption and integration has a cost though.
In a high-volume production context, it may make sense to customize the PIR solution with a design-to-cost approach, going for a specific assembly of pyro-electric sensor element, post-processing and

Fresnel lens, looking for an optimized, application-specific balance between target power consumption and sensor cost

12. Programming / Debugging

> GAP8:
Code can be downloaded into GAP8 internal RAM or into the HyperBus Memory present on GAPmod through its JTAG interface. This is done using the **standard GAP8 SDK**, please refer to its documentation *[Ref.4]*.

The SDK uses OpenOCD, which means any OpenOCD JTAG probe should be usable (at the time of writing, probes from Olimex and Segger have been successfully tested).
GAPPoc features a 10-pin, 1.27mm pitch JTAG interface, compatible with the standard ARM JTAG-10pin pinout. A JTAG-10<>JTAG-20 converter such as that shown in Figure 3 is required to connect to standard JTAG-20 compatible probes such as those mentioned above.
Specific settings in your Makefile may be required to instructing the SDK about the use of the external probe,refer to SDK documentation.

> NINA BLE Module:
The NINA-B112 module comes pre-loaded with a firmware that supports AT commands, which can be used to select a **proprietary "Serial Port Service"** (a kind of wireless UART replacement) or standard BLE profiles, **or to define and use custom GATT profiles**. This use model does not require any firmware download into the NINA module.
However, if desired, it is also possible to reprogram (and debug) the firmware inside NINA. This can be done using the SWD interface of the Nordic BLE chip inside NINA.

13. Multiplexed Resources – How to use them

10.1. UART Multiplexing Scheme

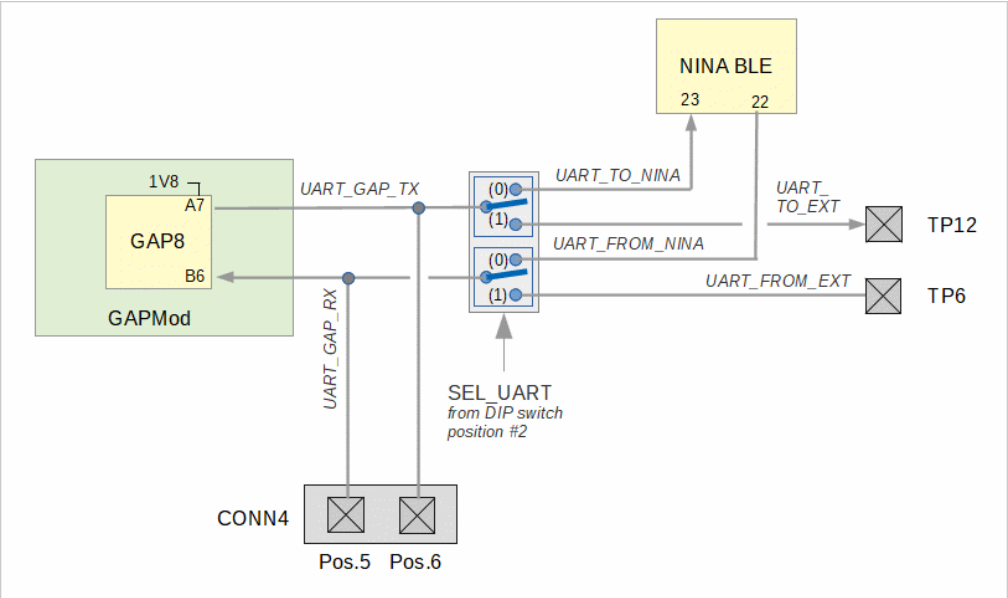


Fig. 5 – UART Sharing scheme on GAPPoc B 2.x

Depending on the position of DIP swithc #2 (SEL_UART), different communication schemes over UART are possible, in particular :
1) GAP8 <> Nina BLE Module (with SEL_UART=0)
2) GAP8 <> external UART-capable device on TP12+TP6 (with SEL_UART=1)
3) Nina BLE <> UART-capable device on CONN4 positions #5 & #6
(with SEL_UART=0 & GAP8 UART I/Os in high-Z state so they don't interfere)
The external "UART capable device" may for example be a PC running a serial terminal program (CuteCom, PUTty…).

In cases (1) and (2), CONN4 can be used to monitor the UART signal waveforms and data stream with an oscilloscope or a logic analyzer.

10.3. Using the Status LED (Green LED, LED3)

The on-board green status LED can be controlled from the GPIO available on GAP8 pin A3. However:
> by default, this feature is disabled, and the LED is not driven. In that mode, pin A3 can be freely used to interact with the outside world through position 2 of connector CONN3.
> If the user closes positions #1 and #6 of the mini-DIP switch (cf. Section 4), then LED3 is driven from GAP8 pin A3. In this mode, the user should not connect anything to position 2 of connector 3 to avoid any conflict.

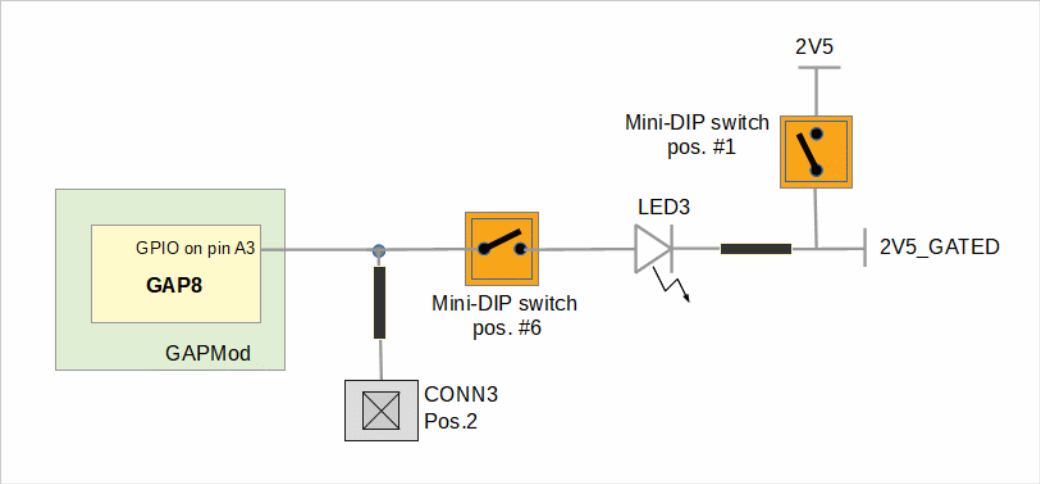


Fig.6 – Sharing of GAP8 pin A3: external connector vs. on-board user LED

14. Board I/Os: Connector Pin Assignments

Note*: different I/Os may use different logic levels, depending on what partition of GAP8's I/O ring they belong to. See GAP8's and GAPmod's datasheets [Ref.1].*

Connector CONN4:
Pos. #1 – **1V8_SAFE_VDDIO from on-board DC-DC**
Pos. #2 – GAP8 pin **B11** [TIMER/GPIO– *see GAP8 datasheet*] – *Caution: shared w/ STM8 if STM8 programmed*
Pos. #3 – GAP8 pin **B13** [GPIO] – *Caution: shared w/ STM8 if STM8 programmed*
Pos. #4 – **3V6_EXT** typ.3.6V from Battery to GAP8 and on-board DC-DC converters
Pos. #5 – **UART_GAP_RX_I** (*)
Pos. #6 – **UART_GAP_TX** (*)
Pos. #7 – **GND**
Pos. #8 – **STM8_WAKE_UP** [routed to always-on STM8 input and usable as system wake up signal with appropriate firmware]
(*) Refer to section 13 on Resource Sharing

Connector CONN3:
Pos. #1 – **1V8_CAM_VDDIO** from on-board DC-DC
Pos. #2 – GAP8 pin **A3** (*) [SPI/GPIO – *see GAP8 datasheet*]
Pos. #3 – GAP8 pin **B3** [SPI/GPIO]
Pos. #4 – GAP8 pin **A4** [SPI/GPIO]
Pos. #5 – GAP8 pin **B4** [SPI/I2C/GPIO]
Pos. #6 – GAP8 pin **A5** [SPI/I2C/GPIO]
Pos. #7 – **GND**

Pos. #8 – GAP8 pin **A13** [TIMER/GPIO]
(*) Also refer to section 13 on Resource Sharing

JTAG Connector CONN5:
Pos. #1 – **1.8V** from on-board DC-DC
Pos. #2 – **JTAG_TMS**
Pos. #3 – **GND**
Pos. #4 – **JTAG_TCK**
Pos. #5 – **GND**
Pos. #6 – **JTAG_TDO**
Pos. #7 – **NC/SWIM** [*Not Connected*]
Pos. #8 – **JTAG_TDI**
Pos. #9 – **NC**
Pos. #10 – **NRESET** [system reset]

REFERENCES

[Ref.1] - GAPmod Datasheet and Schematic – Available from GreenWaves Technologies
GAP8 Datasheet "*GAP8 Hardware Reference Manual*" – available from *greenwaves-technologies.com*

[Ref.2] – "User Guide, ThermEye-b90 & ThermEye-b120", Lynred (formerly ULIS)

[Ref.3] - uBlox NINA-B112 Datasheet
"NINA-B1 Series – stand-alone Bluetooth low energy modules – data sheet"
https://www.u-blox.com/sites/default/files/NINA-B1_DataSheet_%28UBX-15019243%29.pdf

[Ref.4] - GreenWaves GAP8 SDK & Manuals: greenwaves-technologies.com/en/sdk/

[Ref.5] - OLIMEX ARM-USB-OCD-H USB to JTAG/RS232 converter
https://www.olimex.com/Products/ARM/JTAG/ARM-USB-OCD-H/
ARM JTAG 20-pin/2.54mm pitch to 10-pin/1.27mm pitch converter (multiple vendors)

DOCUMENT HISTORY

Jan-2020 (XC):
Initial drafts

Rel.1.0, Mar-2020 (XC):
Initial Release
Lower maximum allowed voltage from battery to 3.6V.

Rel.1.1, Mar-2020 (XC):
Update to reflect the change of Nina module supply scheme – now on dedicated LDO
+ now using DIP switch position 5

Rel.1.2, Apr-2020 (XC):
Clarify that GAP_B11 and _B13 available on connectors are GPIOs shared w/ STM8

Rel.1.3, Sep-2020 (XC):
Reflect evolution from GAPPoc B 2.2 to GAPPoc B 2.3 – a few modifications esp. around acceptable voltage range on JST connector

Rel.1.4, Dec-2020 (XC):
Minor editing to mention GAPPoc B 2.4 along with 2.3

