

Based on Nina-B1 spec:

- > Dual (R+YG) LED :
 - EDM IDLE: Green
 - Cmd mode IDLE: Orange
 - Connecting: Red
 - Connected: Off
- > Single (G) LED:
 - Connecting or Connected: ON
 - Idle: OFF

NINA_LED_EN

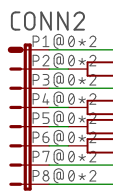
Drive HIGH to enable LEDs,
LOW or high-Z
to cut power consumption

Biased for ~5mA @Vfmax=2.2V(G)/2.1V(R)

GAP8 allowed to drive (as SW1)
at BLE reset,
then BLE is driving (as LED_G)

R selected for 2mA @Vfmax=2.1V

- R13 100R
- R14 100R
- R15 100R
- R16 100R

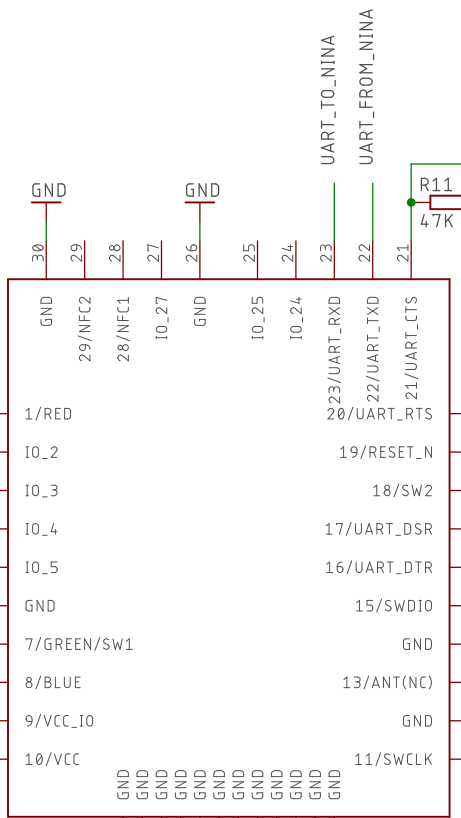


BG120-08-xx

!! MIGHT NEED SOME ADDITIONAL PROVISIONS FOR FULL PIN COMPATIBILITY WITH NINA WIFI MODULES !!!



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NINA_CTS_CONN

U8

NINA_SWCK

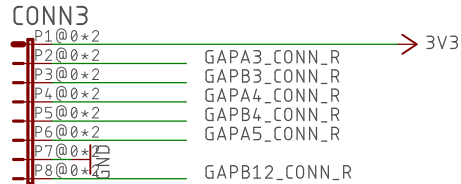
NINA_SWCK

NINA-B1

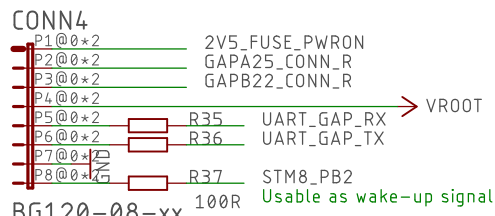
Back-up, for debug

Back-up, for debug

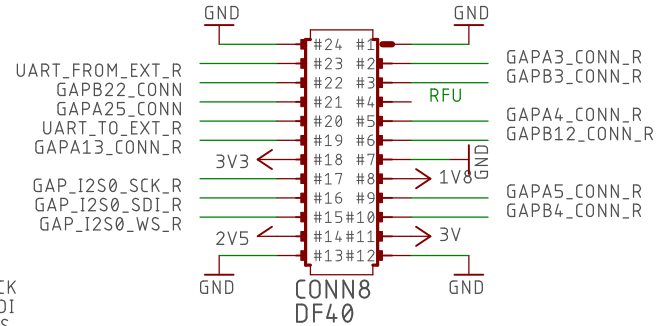
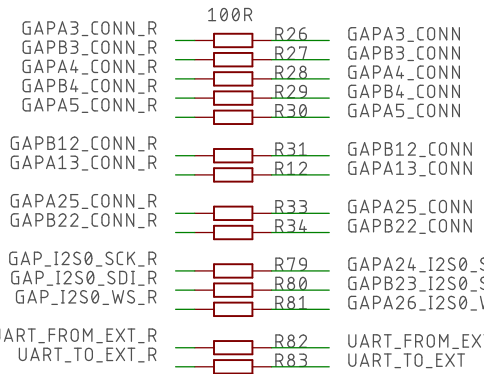
1 2 3 4 5 6



BG120-08-xx



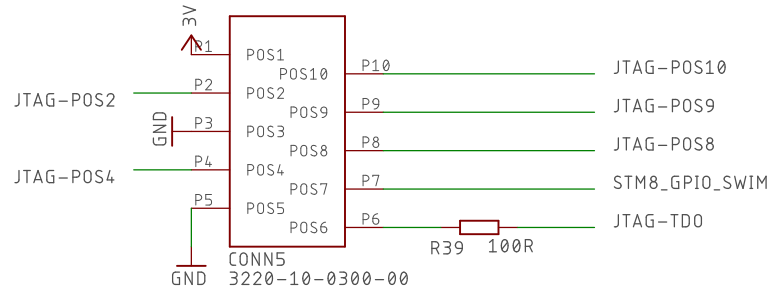
BG120-08-xx



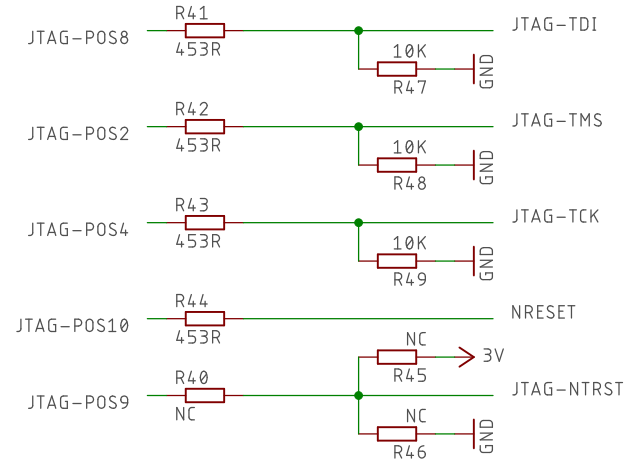
Provides SPI, I2C, (UART), Timers, GPIO to daughter board

- SPI1 on GAP_A4,B3,A5,B4 (also I2C1 but I2C1 also on pins to CIS)
- Timer/PWM on pins GAP_A13, B12
- I2C0 on GAP_B22, A25
- I2S0 on GAP_A24, A26, B23
- UART on GAP_B6, A7 (but shared)

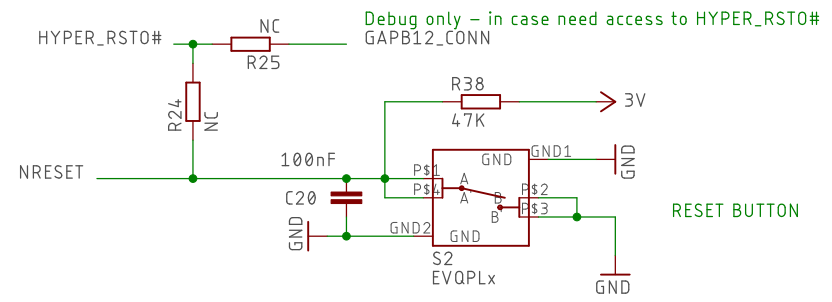
Also usable as GPIO except I2S0 & I2C0



JTAG Connector
NOTE - This pinning is intended to be compatible with TagConnect TC2050 JTAG-ARM-20 to JTAG-ARM-10 converter



Normally, not driving JTAG-NTRST at GAP8 input is OK. Provision back-up structure though.



RESET BUTTON

Connectors and Switches

1 2 3 4 5 6

A

B

C

D

A

B

C

D

1 2 3 4 5 6

A

B

C

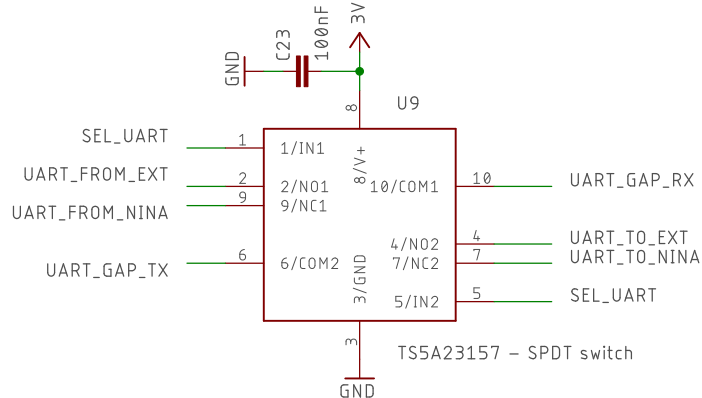
D

A

B

C

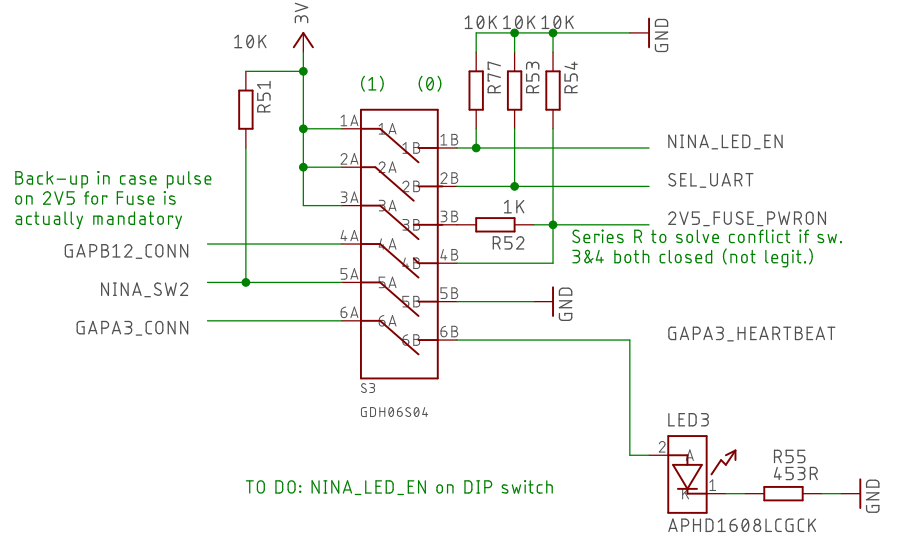
D



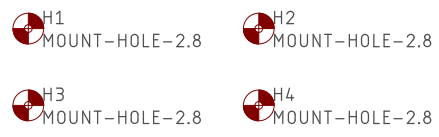
IF EXT SOURCE can be disconnected or is H-Z capable, then CONNx can be used not only as TP but also to plug UART i/f to talk with GAP8

NB:
 - Slight static power consumption when switch is closed (3V/10K=300uA)
 - Default switch position = (0) / Open - for normal use case

Open/closed switches :
 1: n/a
 2: selects UART for NINA or for Conn.
 3: selects if Fuse Power Enable is Off/forced on
 4: selects if Fuse Power Enable is controlled from GPIO (dont select Forced0n + GPIO-based)
 5: selects normal or bootload/restore modes at NINA startup
 6: selects if GAP_A3 is available as GPIO on connector or is recycled as heartbeat LED



One non-plated hole in each corner

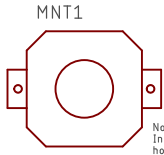


Fiducials



Switches & Electro-mechanics	
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1 2 3 4 5 6



No electrical connection.
Instantiate to have keepouts and
holes from associated symbol in layout.

18mm interaxis M12 S-mount

A

A

B

B

C

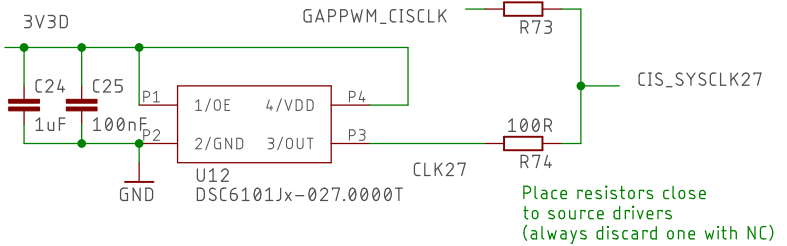
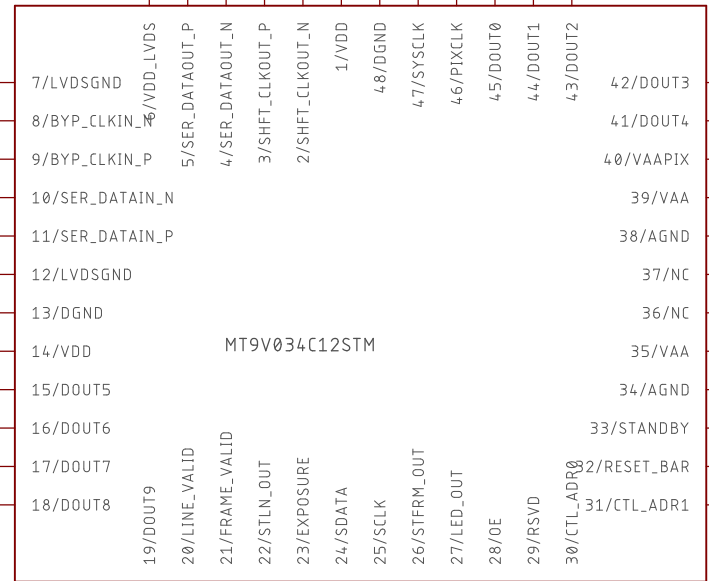
C

D

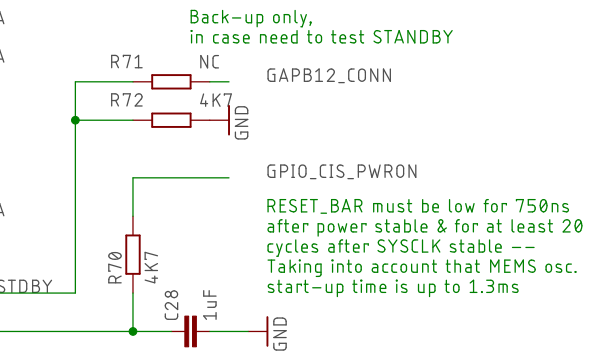
D

No stereoscopy

- DOUT2 R56 100R CIS_D2_CPI_D0
- DOUT3 R57 100R CIS_D3_CPI_D1
- DOUT4 R58 100R CIS_D4_CPI_D2
- DOUT5 R59 100R CIS_D5_CPI_D3
- DOUT6 R60 100R CIS_D6_CPI_D4
- DOUT7 R61 100R CIS_D7_CPI_D5
- DOUT8 R62 100R CIS_D8_CPI_D6
- DOUT9 R63 100R CIS_D9_CPI_D7
- VSYNC R64 100R CIS_VSYNC
- HSYNC R65 100R CIS_HSYNC
- PCLK R66 100R CIS_PCLK

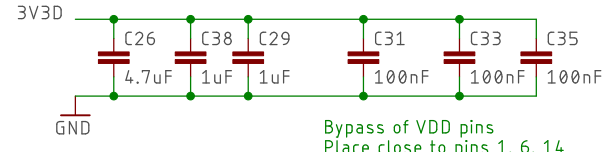


Place resistors close to source drivers (always discard one with NC)

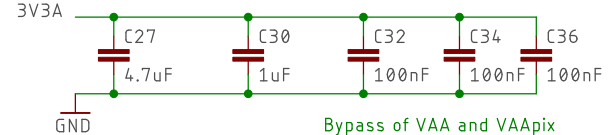


Back-up only, in case need to test STANDBY

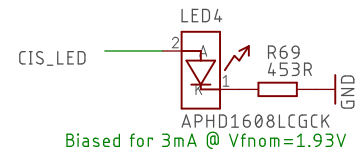
RESET_BAR must be low for 750ns after power stable & for at least 20 cycles after SYCLK stable -- Taking into account that MEMS osc. start-up time is up to 1.3ms



Bypass of VDD pins Place close to pins 1, 6, 14



Bypass of VAA and VAAPIX Place close to pins 35, 39, 40



Biased for 3mA @ Vfnom=1.93V

Image Sensor
Use common Ground Plane but partition layout into an analogue region (no dig. signal over it) and a digital region

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