GAPMod 2.x

DOCUMENTATION

Rel. 2.0
13-Jan-2019

CONTENTS

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Preamble - GAPMod 2.0 vs. GAPMod 1.x

GAPMod 2.0 is a lower cost version of GAPMod1.2.
The external Flash+RAM on HyperBus has been replaced by an external Flash and external RAM on QPI (Quad-SPI) bus.
In addition, some non-essential hardware that had been provisioned on GAPMod 1.x has been removed.
Pin numbering has been rationalized but pin compatibility is mostly maintained (see dedicated section).

1. Introduction

GAPMod is a core module architectured around GreenWaves Technologies' GAP8 chip, an ultra-low power Application Processor for the IoT (*Ref[1]).*
GAPMod is intended to facilitate and speed up development of applications around GAP8.
It packs on a small board (26mmx36mm) the "invariant" part of any application based on GAP8 (GAP8 chip, external Flash+RAM memory, associated decoupling caps, crystal oscillator, passives for internal DC-DC, etc.). This core hardware happens to also be, in many use cases, the most demanding part of the overall design in terms of precautions to take and in terms of required PCB technology.

With GAPMod, an application PCB designer can simply drop the module in his/her design and rely on comparatively relaxed Design Rules and reasonably priced PCB technology for his/her own application-specific motherboard.

2. Board Description

GAPMod comes in the form of a 4-layer PCB to be assembled using SMT (Surface Mount Technology) on a target board. All components therefore sit on one side while the other side bears the SMT pads.

All GAP8 I/Os that are not dedicated to interconnecting chips present on GAPMod are made available to the target application board as GAPMod I/Os. For maximum flexibility, power supplies are also to be provided by the application board, with the exception of that dedicated to the on-chip crystal oscillator.
Figure 1 highlights the major parts that constitute GAPMod, while Figure 2 details physical dimensions of the board and location plus size of its I/O pads.

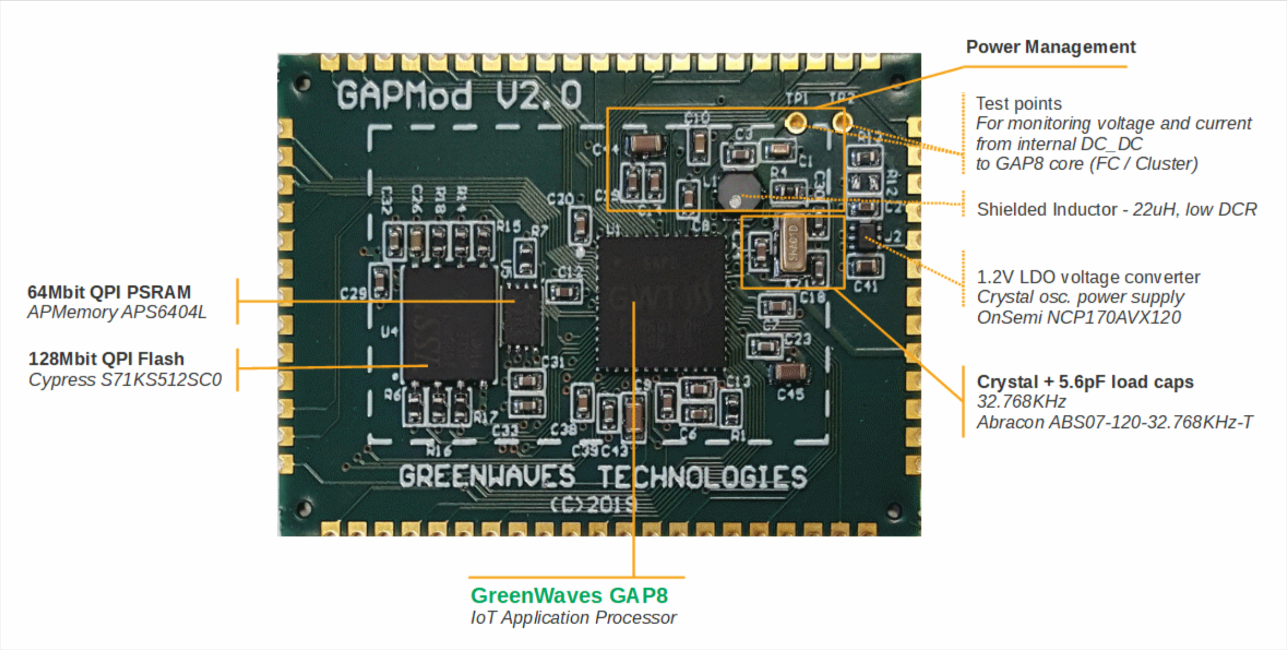
GAPMod V2.0
GREENWAVES TECHNOLOGIES
(C) 2019
Power Management
Test points
For monitoring voltage and current from internal DC_DC to GAP8 core (FC / Cluster)
Shielded Inductor - 22uH, low DCR
1.2V LDO voltage converter
Crystal osc. power supply
OnSemi NCP170AVX120
Crystal + 5.6pF load caps
32.768KHz
Abracon ABS07-120-32.768KHz-T
64Mbit QPI PSRAM
APMemory APS6404L
128Mbit QPI Flash
Cypress S71KS512SC0
GreenWaves GAP8
IoT Application Processor

Fig. 1: Anatomy of GAPMod 2.0

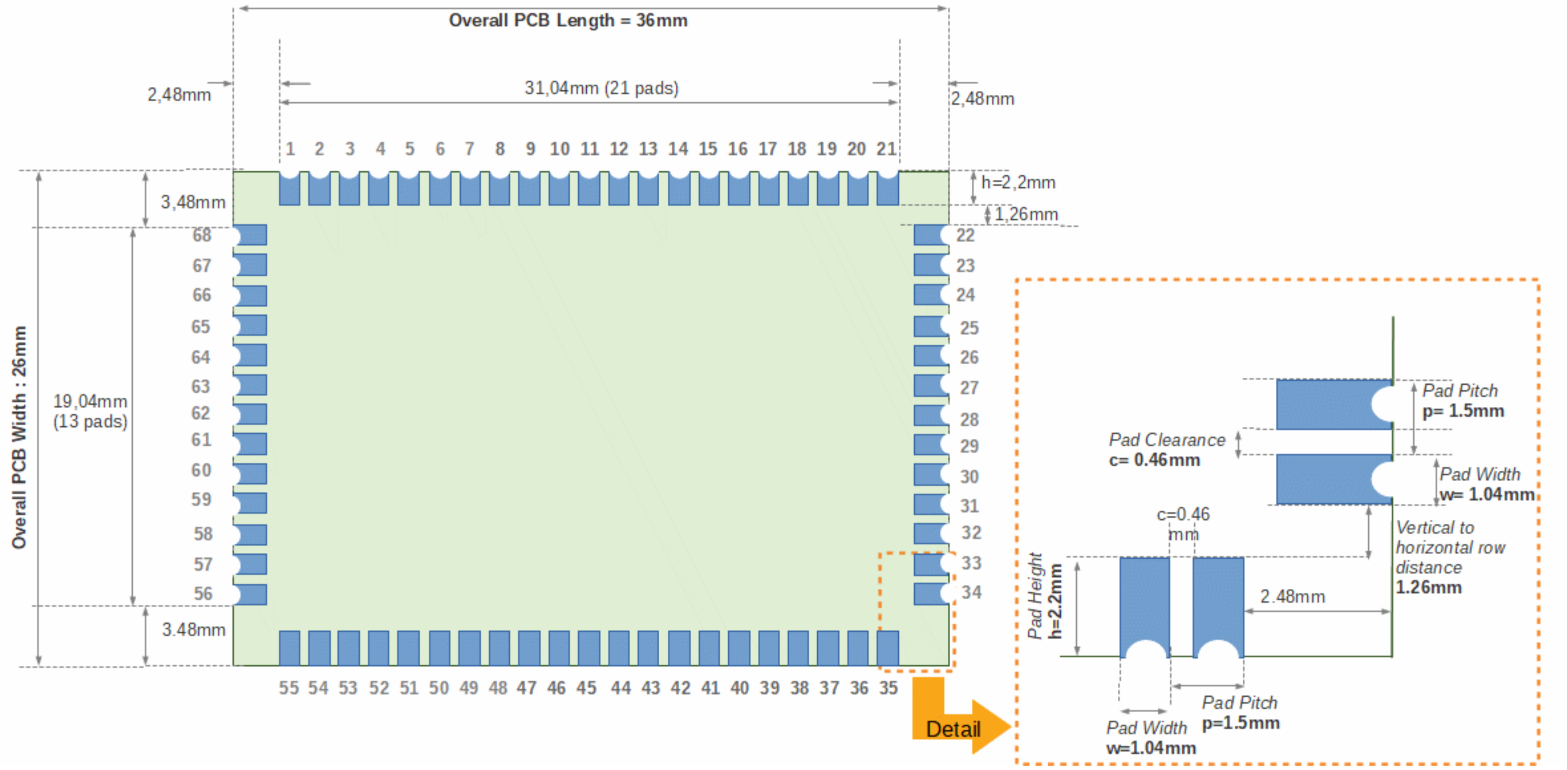

Fig. 2: GAPMod 2.0 Physical Information, TOP (see-through) View

3. GAP8

Central to the board is the GAP8 chip, an ultra-low power Application Processor for the IoT, bringing intelligence at network edge. GAP8 brings the ability to analyze and classify data from sensors (images, sounds, vibrations etc.) at very low cost and very low power, by extracting from sensor data condensed, meaningful information which can then be sent efficiently over a network.
GAP8 consists on an MCU-like part (a core plus standard peripherals), a processing intensive part (8 identical parallel cores plus a hardware accelerator specialized in Convolutional Neural Network operations), with on-chip L1 and L2 RAM and a specialized DMA. The cores are 32-bit RISC-V enhanced with specialized instructions.
Refer to the GAP8 Product Brief and Datasheet *(Ref.1])* for details.

4. On-board power management

Refer to Fig. 3 for a graphical illustration of power management on GAPMod.
As mentioned earlier, most power supplies are to be provided by the application board in the sake of flexibility.
However, the crystal oscillator is powered on-board. By default it is powered off VREG, the 0.8V-1.2V voltage generated by the internal DC-DC converter – this is the lowest cost approach. A dedicated 1.2V LDO is also provisioned on-board, to provide a potentially cleaner and more stable voltage; also in case operating the crystal oscillator at 0.8V (limit of specification) in sleep mode does not work as reliably as expected (not fully characterized at the time of writing). Selection is through an assembly option (populating or not some parts).

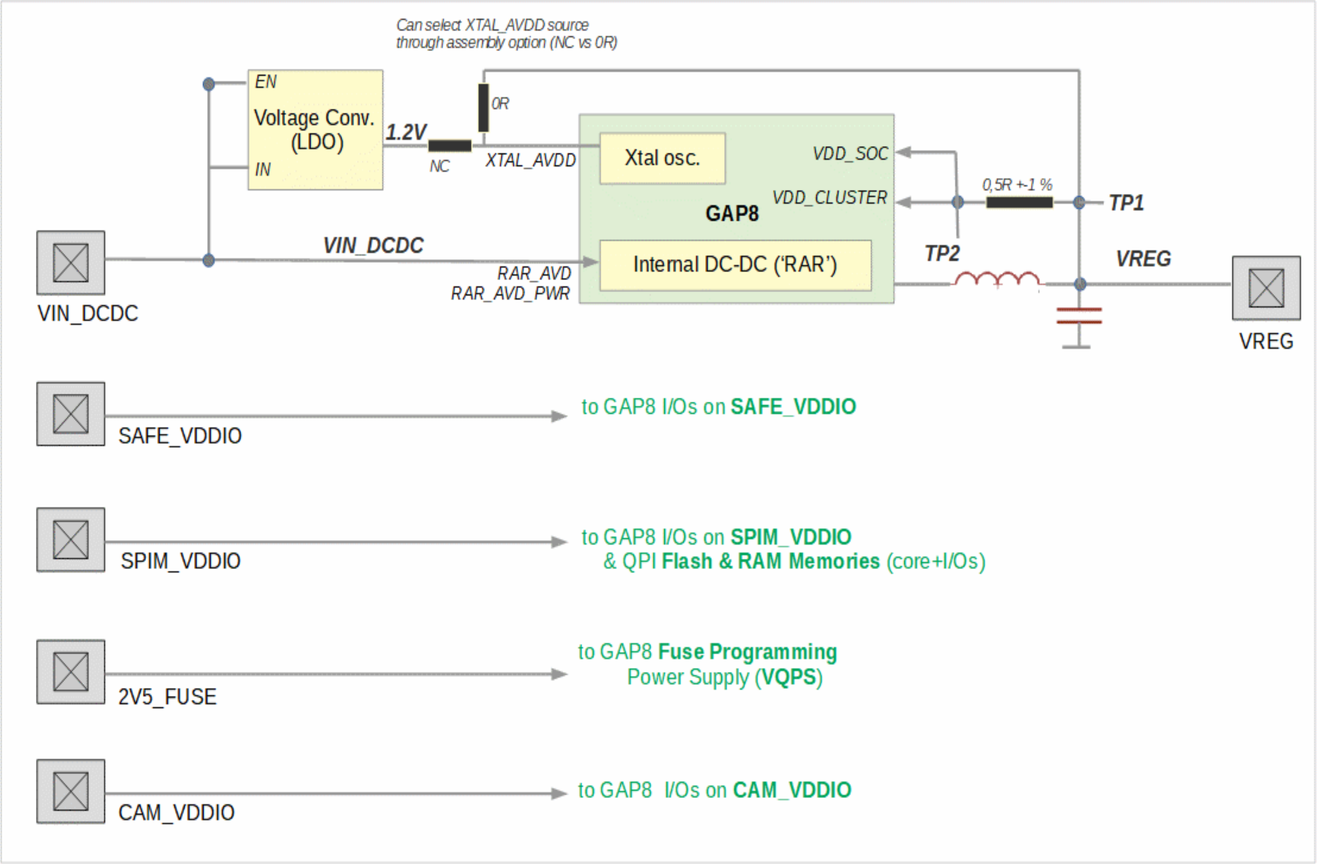

Fig. 3 – On-board power supply generation and control (notional)

– Test Points / Power Supply Monitoring –

Two testpoints, TP1 and TP2, are provided to monitor supply voltage and supply current drawn by the "SoC" part (a.k.a FC, Fabric Controller) and the "Cluster" part of the GAP8 chip (i.e. full digital core, excluding I/Os and oscillator).

The current flows through a 0.5 ohm (+-1%) sense resistor placed on the current path between TP1 and TP2. Therefore the current consumption (in mA) is twice (2x) the value of the measured voltage drop (in mV) since I=U/R. The sense resistance is deliberately small to avoid severe supply voltage fluctuations when there are significant instantaneous current changes.

The current consumption is measured at output of the DC-DC converter. The efficiency of DC-DC conversion will determine how this translate as actual power drawn by GAP8 (SOC aka FC +Cluster) at system level.

> the regulated voltage VREG is made available on an I/O pad of GAPMod. This allows monitoring VREG; it could for example be used by external hardware to detect if GAPMod is in Sleep mode without relying on another specific signal, as:
- in normal mode, VREG may range from 1.0V to 1.2V
- in sleep mode, the internal DC-DC switches to LDO mode and provides VREG=0.8V.

5. Flash and RAM Memories

GAPMod 2.x implements a 128Mbit Flash Memory (ISSI IS25WP128_JKLE on initial batch, possibly equivalent chip on next ones) and a 64Mbit pseudo-static RAM (APMemory APS6404L-SQRH-ZR), both on the QPI (Quad-SPI) bus. They require 1.8V nominal power supply (1,7V min, 1,95V max).

The QPI memory bus is on the SPIM0 interface of GAP8 (see datasheet *[Ref.1).* The Flash is addressed by asserting SPIM0_CS0 (pin B8) while the RAM is addressed by asserting SPIM0_CS1 (pin A8).

6. Programming / Debugging

Code can be downloaded into GAP8 internal RAM or into the Flash Memory present on GAPMod through its JTAG interface. This is done using the **standard GAP8 SDK**, please refer to its documentation *[Ref.2].*

7. GAPMod I/O Signal Assignements

Please refer to Table "GAPMod I/Os" (provided as a separate spreadsheet (*[Ref.3]*).
Pin compatibility with GAPMod1.2 is mostly preserved. The role of a few I/Os has been modified but a board that worked with GAPMod1.2 should accept GAPMod2.0 – with the possible exception of UART interface. On GAPMOd1.2, UART signals (natively referenced to SPIM_VDDIO on GAP8) were level shifted to SAFE_VDDIO, this is no longer the case on GAPMod2.0, where they remain referenced to SPIM_VDDIO.

REFERENCES

Ref[1] -
Product Brief "*GAP8 IoT Application Processor*" – available from *greenwaves-technologies.com*
DataSheet "*GAP8 Hardware Reference Manual*" – available from *greenwaves-technologies.co*m

Ref[2] -
GreenWaves GAP8 SDK & Manuals :   *greenwaves-technologies.com/en/sdk/*

Ref[3] -
Functional Definition of GAPMod 2.x I/Os :
Spreadsheet *GAPMod_v2.x_IO_Definition.xlsx* available from GreenWaves
Pin # on GAPMod vs. connection of GAPMod (e.g. Pin ID on GAP8 if relevant) and brief description of intended usages.

DOCUMENT HISTORY

Rel.1.0 – Aug.2019 (XC)
Creation (starting from Rel.2.1 of GAPMod1.x documentation)

Rel.1.1 – Sep.2019 (XC)
Add information about SPI pin mapping to Flash and RAM

Rel.2.0 – Jan.2019 (XC)
Fix remaining issues and release publicly