

GAP8 POWER SUPPLY DECOUPLING

HYPERMEM DECOUPLING

!!! Follow guidelines of Cypress's AN 211622 "HyperFlash and HyperRAM Layout Guide" !!!

GAP8 & Memory
GAPMOD-V1.2_SchemOnly
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3V_1V8_MEMCORE_MEMIO

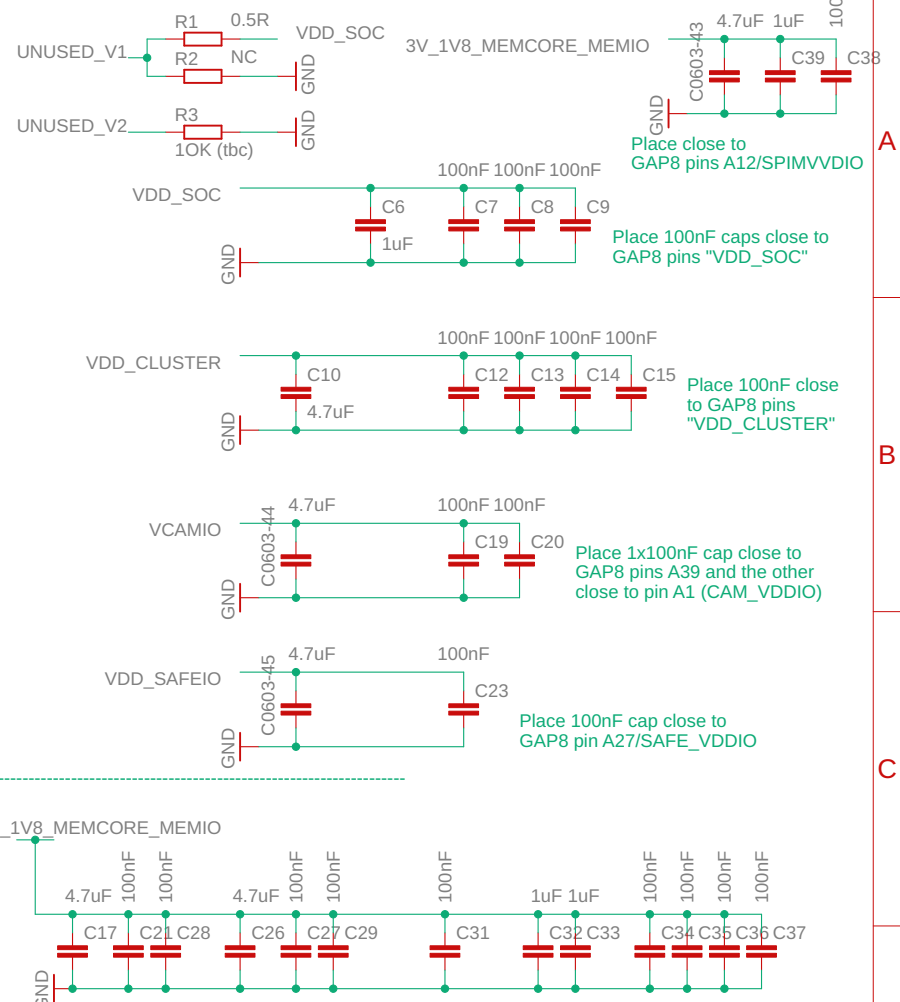
U1
GAP8

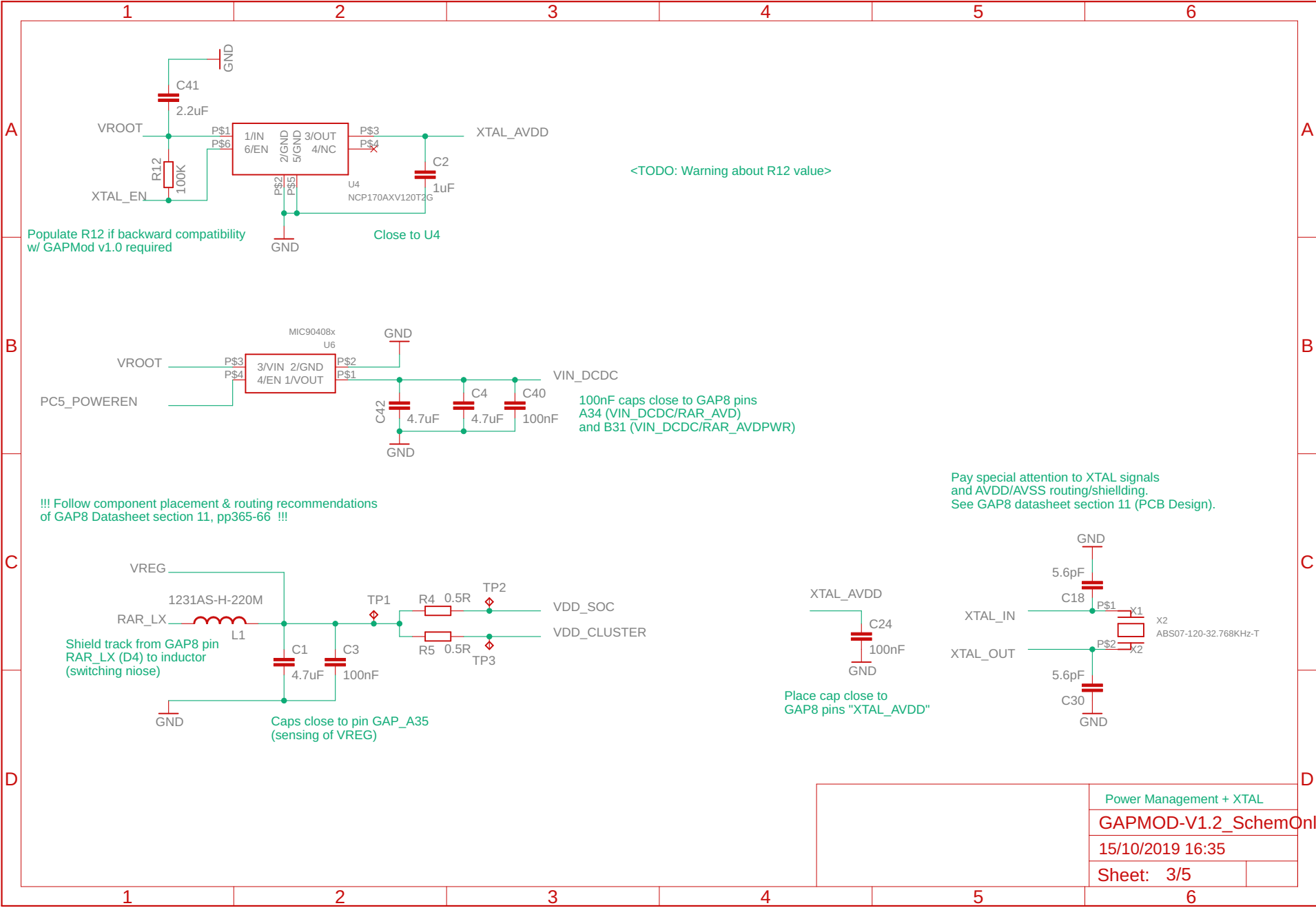
U2
S71K5512SC0B/S71KL256SC0B/S71KL512SC0B

TBD - Add pull-up on Mem CS ??

B5	B5/RFU	B4/VCC	D3/DQ0	D3	HYPER_DQ0
C5	C5/RFU	D1/VCCQ	D2/DQ1	D2	HYPER_DQ1
		E4/VCCQ	C4/DQ2	C4	HYPER_DQ2
			D4/DQ3	D4	HYPER_DQ3
A4	A4/RESET#		D5/DQ4	D5	HYPER_DQ4
			E3/DQ5	E3	HYPER_DQ5
C2	C2/CS1#	B3/VSS	E2/DQ6	E2	HYPER_DQ6
A3	A3/CS2#	E5/VSSQ	E1/DQ7	E1	HYPER_DQ7
		C1/VSSQ			
			C3/RWDS	C3	HYPER_RWDS
			A5/INT#	A5	HYPER_INT#
			A2/RSTO#	A2	HYPER_RSTO#

INT# and RSTO# are not speed-critical





Populate R12 if backward compatibility w/ GAPMod v1.0 required

<TODO: Warning about R12 value>

Close to U4

!!! Follow component placement & routing recommendations of GAP8 Datasheet section 11, pp365-66 !!!

100nF caps close to GAP8 pins A34 (VIN_DCDC/RAR_AVDD) and B31 (VIN_DCDC/RAR_AVDPWR)

Pay special attention to XTAL signals and AVDD/AVSS routing/shielding. See GAP8 datasheet section 11 (PCB Design).

Shield track from GAP8 pin RAR_LX (D4) to inductor (switching noise)

Caps close to pin GAP_A35 (sensing of VREG)

Place cap close to GAP8 pins "XTAL_AVDD"

Power Management + XTAL

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1

2

3

4

5

6

A

A

B

B

C

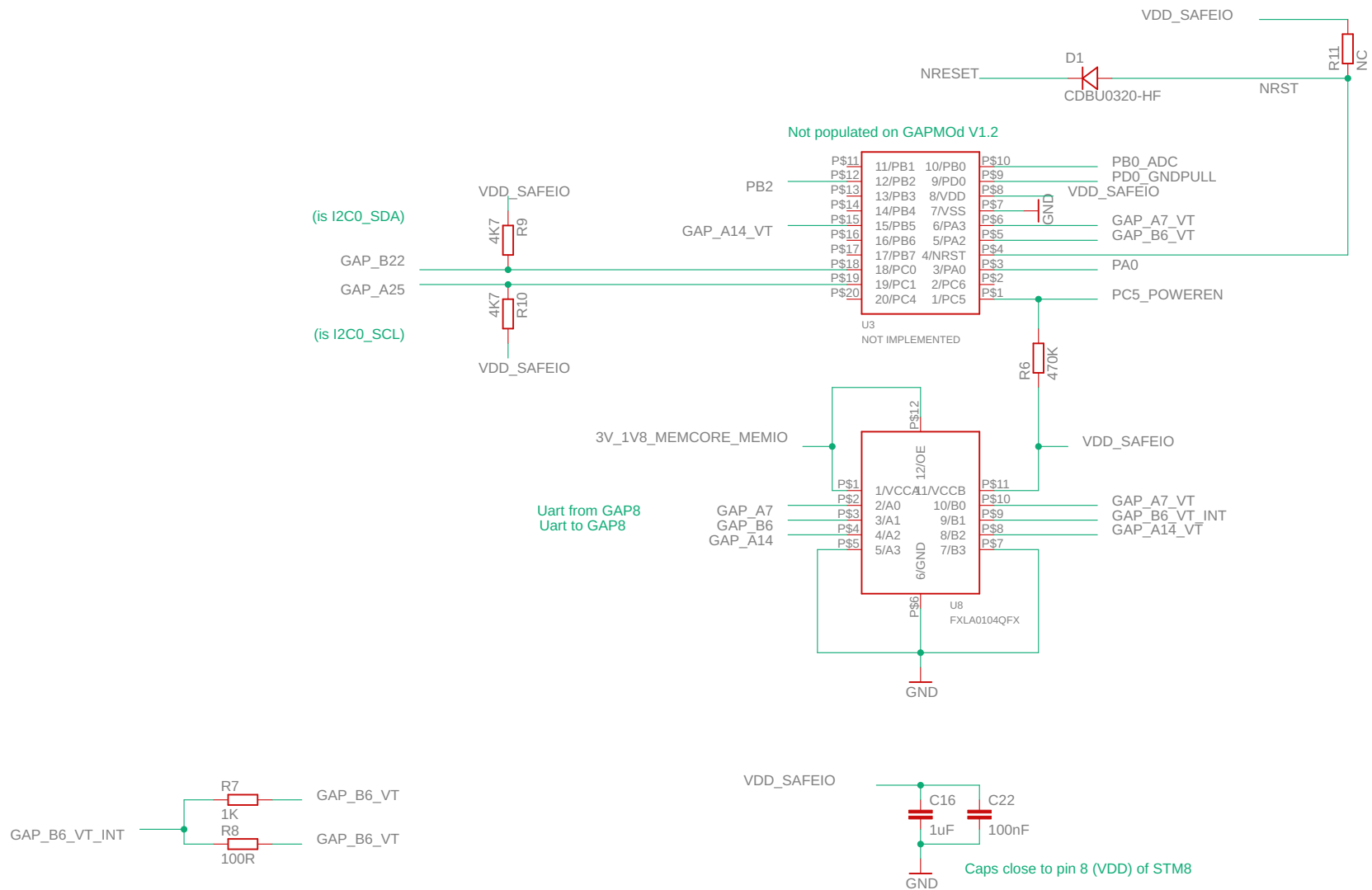
C

D

D

E

E



STM8 -
UART voltage translation & muxing

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