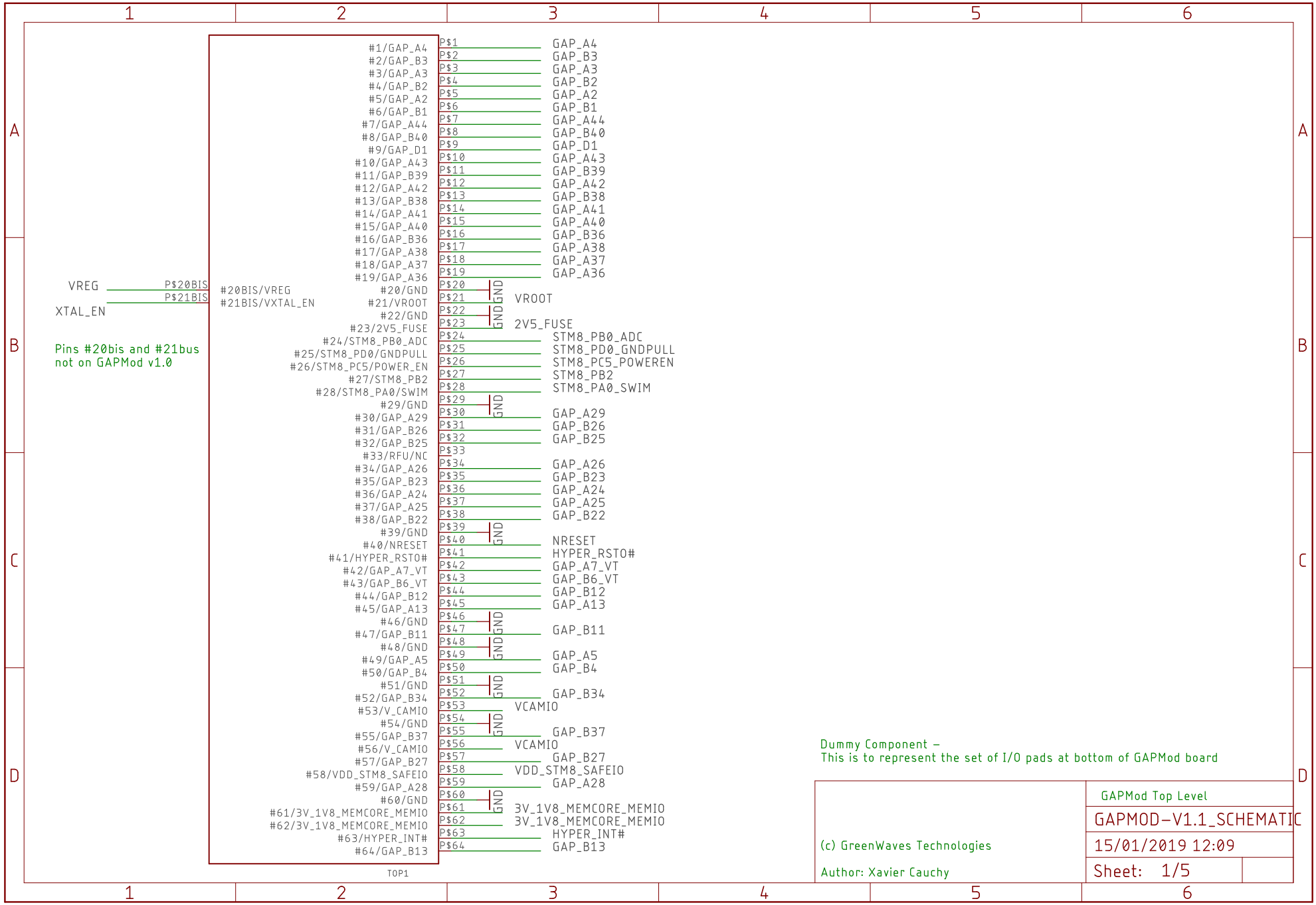
1
2
3
4
5
6
A
B
C
D
VREG
XTAL_EN
P$20BIS
P$21BIS
Pins #20bis and #21bus
not on GAPMod v1.0
#1/GAP_A4
#2/GAP_B3
#3/GAP_A3
#4/GAP_B2
#5/GAP_A2
#6/GAP_B1
#7/GAP_A44
#8/GAP_B40
#9/GAP_D1
#10/GAP_A43
#11/GAP_B39
#12/GAP_A42
#13/GAP_B38
#14/GAP_A41
#15/GAP_A40
#16/GAP_B36
#17/GAP_A38
#18/GAP_A37
#19/GAP_A36
#20BIS/VREG
#21BIS/VXTAL_EN
#20/GND
#21/VROOT
#22/GND
#23/2V5_FUSE
#24/STM8_PB0_ADC
#25/STM8_PD0/GNDPULL
#26/STM8_PC5/POWER_EN
#27/STM8_PB2
#28/STM8_PA0/SWIM
#29/GND
#30/GAP_A29
#31/GAP_B26
#32/GAP_B25
#33/RFU/NC
#34/GAP_A26
#35/GAP_B23
#36/GAP_A24
#37/GAP_A25
#38/GAP_B22
#39/GND
#40/NRESET
#41/HYPER_RSTO#
#42/GAP_A7_VT
#43/GAP_B6_VT
#44/GAP_B12
#45/GAP_A13
#46/GND
#47/GAP_B11
#48/GND
#49/GAP_A5
#50/GAP_B4
#51/GND
#52/GAP_B34
#53/V_CAMIO
#54/GND
#55/GAP_B37
#56/V_CAMIO
#57/GAP_B27
#58/VDD_STM8_SAFEIO
#59/GAP_A28
#60/GND
#61/3V_1V8_MEMCORE_MEMIO
#62/3V_1V8_MEMCORE_MEMIO
#63/HYPER_INT#
#64/GAP_B13
P$1 GAP_A4
P$2 GAP_B3
P$3 GAP_A3
P$4 GAP_B2
P$5 GAP_A2
P$6 GAP_B1
P$7 GAP_A44
P$8 GAP_B40
P$9 GAP_D1
P$10 GAP_A43
P$11 GAP_B39
P$12 GAP_A42
P$13 GAP_B38
P$14 GAP_A41
P$15 GAP_A40
P$16 GAP_B36
P$17 GAP_A38
P$18 GAP_A37
P$19 GAP_A36
P$20 GND
P$21 VROOT
P$22 GND
P$23 2V5_FUSE
P$24 STM8_PB0_ADC
P$25 STM8_PD0_GNDPULL
P$26 STM8_PC5_POWEREN
P$27 STM8_PB2
P$28 STM8_PA0_SWIM
P$29 GND
P$30 GAP_A29
P$31 GAP_B26
P$32 GAP_B25
P$33
P$34 GAP_A26
P$35 GAP_B23
P$36 GAP_A24
P$37 GAP_A25
P$38 GAP_B22
P$39 GND
P$40 NRESET
P$41 HYPER_RSTO#
P$42 GAP_A7_VT
P$43 GAP_B6_VT
P$44 GAP_B12
P$45 GAP_A13
P$46 GND
P$47 GAP_B11
P$48 GND
P$49 GAP_A5
P$50 GAP_B4
P$51 GND
P$52 GAP_B34
P$53 VCAMIO
P$54 GND
P$55 GAP_B37
P$56 VCAMIO
P$57 GAP_B27
P$58 VDD_STM8_SAFEIO
P$59 GAP_A28
P$60 GND
P$61 3V_1V8_MEMCORE_MEMIO
P$62 3V_1V8_MEMCORE_MEMIO
P$63 HYPER_INT#
P$64 GAP_B13
TOP1
Dummy Component –
This is to represent the set of I/O pads at bottom of GAPMod board
(c) GreenWaves Technologies
Author: Xavier Cauchy
GAPMod Top Level
GAPMOD-V1.1_SCHEMATIC
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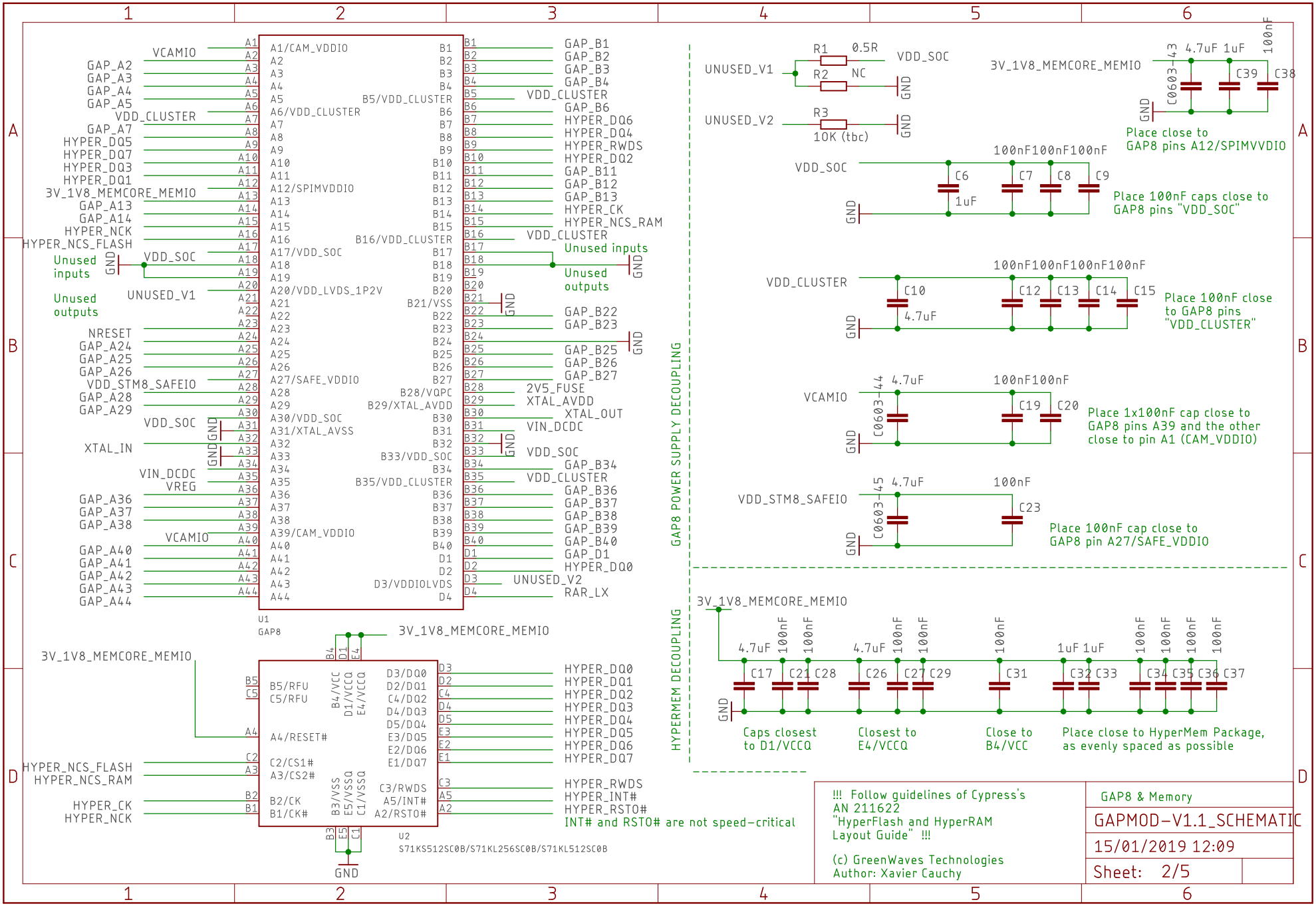
VCAMIO
GAP_A2
GAP_A3
GAP_A4
GAP_A5
VDD_CLUSTER
GAP_A7
HYPER_DQ5
HYPER_DQ7
HYPER_DQ3
HYPER_DQ1
3V_1V8_MEMCORE_MEMIO
GAP_A13
GAP_A14
HYPER_NCK
HYPER_NCS_FLASH
Unused inputs
VDD_SOC
UNUSED_V1
Unused outputs
NRESET
GAP_A24
GAP_A25
GAP_A26
VDD_STM8_SAFEIO
GAP_A28
GAP_A29
VDD_SOC
XTAL_IN
VIN_DCDC
VREG
GAP_A36
GAP_A37
GAP_A38
VCAMIO
GAP_A40
GAP_A41
GAP_A42
GAP_A43
GAP_A44
A1/CAM_VDDIO
A12/SPIMVDDIO
A16/VDD_CLUSTER
A17/VDD_SOC
A20/VDD_LVDS_1P2V
A27/SAFE_VDDIO
A30/VDD_SOC
A31/XTAL_AVSS
A39/CAM_VDDIO
B5/VDD_CLUSTER
B16/VDD_CLUSTER
B21/VSS
B28/VQPC
B29/XTAL_AVDD
B33/VDD_SOC
B35/VDD_CLUSTER
D3/VDDIOLVDS
U1
GAP8
GAP_B1
GAP_B2
GAP_B3
GAP_B4
VDD_CLUSTER
GAP_B6
HYPER_DQ6
HYPER_DQ4
HYPER_RWDS
HYPER_DQ2
GAP_B11
GAP_B12
GAP_B13
HYPER_CK
HYPER_NCS_RAM
VDD_CLUSTER
Unused inputs
Unused outputs
GAP_B22
GAP_B23
GAP_B25
GAP_B26
GAP_B27
2V5_FUSE
XTAL_AVDD
XTAL_OUT
VIN_DCDC
VDD_SOC
GAP_B34
VDD_CLUSTER
GAP_B36
GAP_B37
GAP_B38
GAP_B39
GAP_B40
GAP_D1
HYPER_DQ0
UNUSED_V2
RAR_LX
GAP8 POWER SUPPLY DECOUPLING
3V_1V8_MEMCORE_MEMIO
HYPER_DQ0
HYPER_DQ1
HYPER_DQ2
HYPER_DQ3
HYPER_DQ4
HYPER_DQ5
HYPER_DQ6
HYPER_DQ7
HYPER_RWDS
HYPER_INT#
HYPER_RSTO#
INT# and RSTO# are not speed-critical
HYPER_NCS_FLASH
HYPER_NCS_RAM
HYPER_CK
HYPER_NCK
U2
S71KS512SC0B/S71KL256SC0B/S71KL512SC0B
GND
UNUSED_V1
R1 0.5R
R2 NC
VDD_SOC
UNUSED_V2
R3
10K (tbc)
3V_1V8_MEMCORE_MEMIO
C0603-43
4.7uF 1uF
100nF
C39 C38
Place close to
GAP8 pins A12/SPIMVVDIO
VDD_SOC
100nF100nF100nF
C6 C7 C8 C9
1uF
Place 100nF caps close to
GAP8 pins "VDD_SOC"
VDD_CLUSTER
100nF100nF100nF100nF
C10 C12 C13 C14 C15
4.7uF
Place 100nF close
to GAP8 pins
"VDD_CLUSTER"
VCAMIO
C0603-44
4.7uF
100nF100nF
C19 C20
Place 1x100nF cap close to
GAP8 pins A39 and the other
close to pin A1 (CAM_VDDIO)
VDD_STM8_SAFEIO
C0603-45
4.7uF
100nF
C23
Place 100nF cap close to
GAP8 pin A27/SAFE_VDDIO
HYPERMEM DECOUPLING
3V_1V8_MEMCORE_MEMIO
4.7uF 100nF 100nF
C17 C21 C28
Caps closest
to D1/VCCQ
4.7uF 100nF 100nF
C26 C27 C29
Closest to
E4/VCCQ
100nF
C31
Close to
B4/VCC
1uF 1uF
C32 C33
100nF 100nF 100nF 100nF
C34 C35 C36 C37
Place close to HyperMem Package,
as evenly spaced as possible
!!! Follow guidelines of Cypress's
AN 211622
"HyperFlash and HyperRAM
Layout Guide" !!!
(c) GreenWaves Technologies
Author: Xavier Cauchy
GAP8 & Memory
GAPMOD-V1.1_SCHEMATIC
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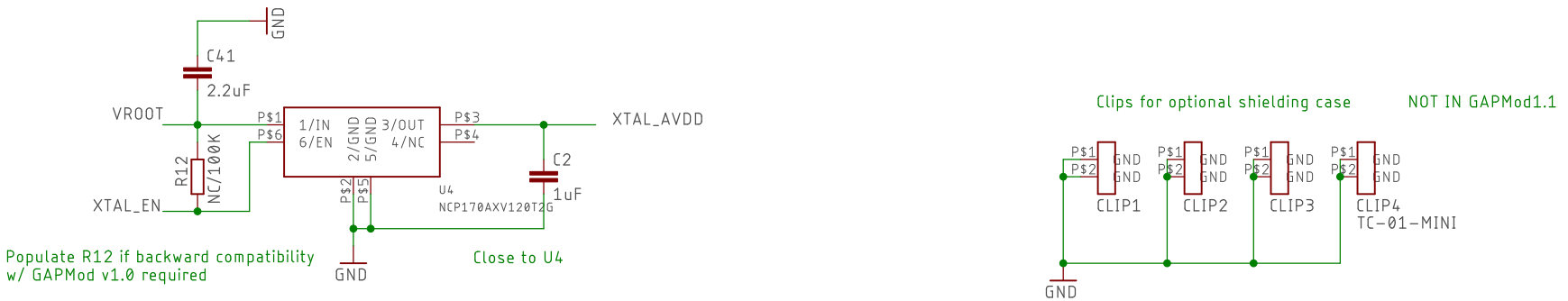
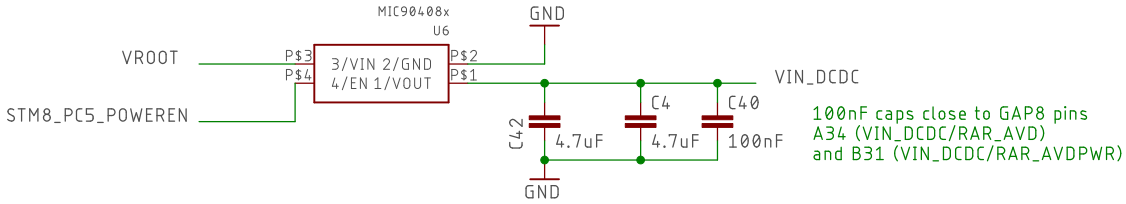
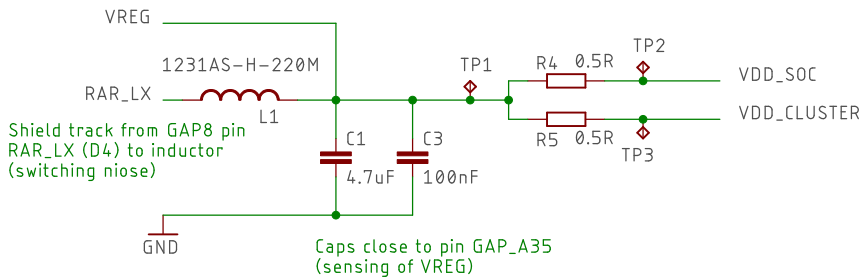
Sheet: 2/5

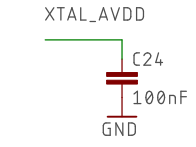


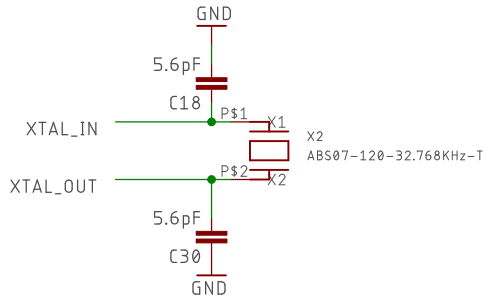


!!! Follow component placement & routing recommendations
of GAP8 Datasheet section 11, pp365-66 !!!



Pay special attention to XTAL signals
and AVDD/AVSS routing/shielding.
See GAP8 datasheet section 11 (PCB Design).





Author: Xavier Cauchy

Power Management + XTAL

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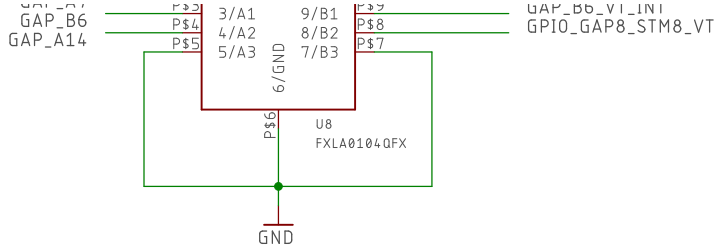
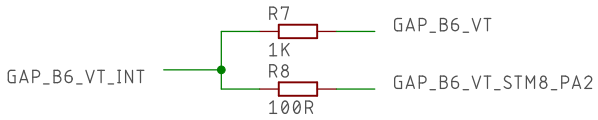
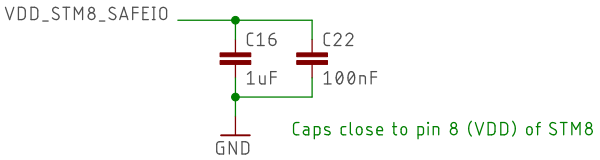
Uart to GAP8







STM8 –
UART voltage translation & muxing

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Document Number:

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Date: 15/01/2019 12:09

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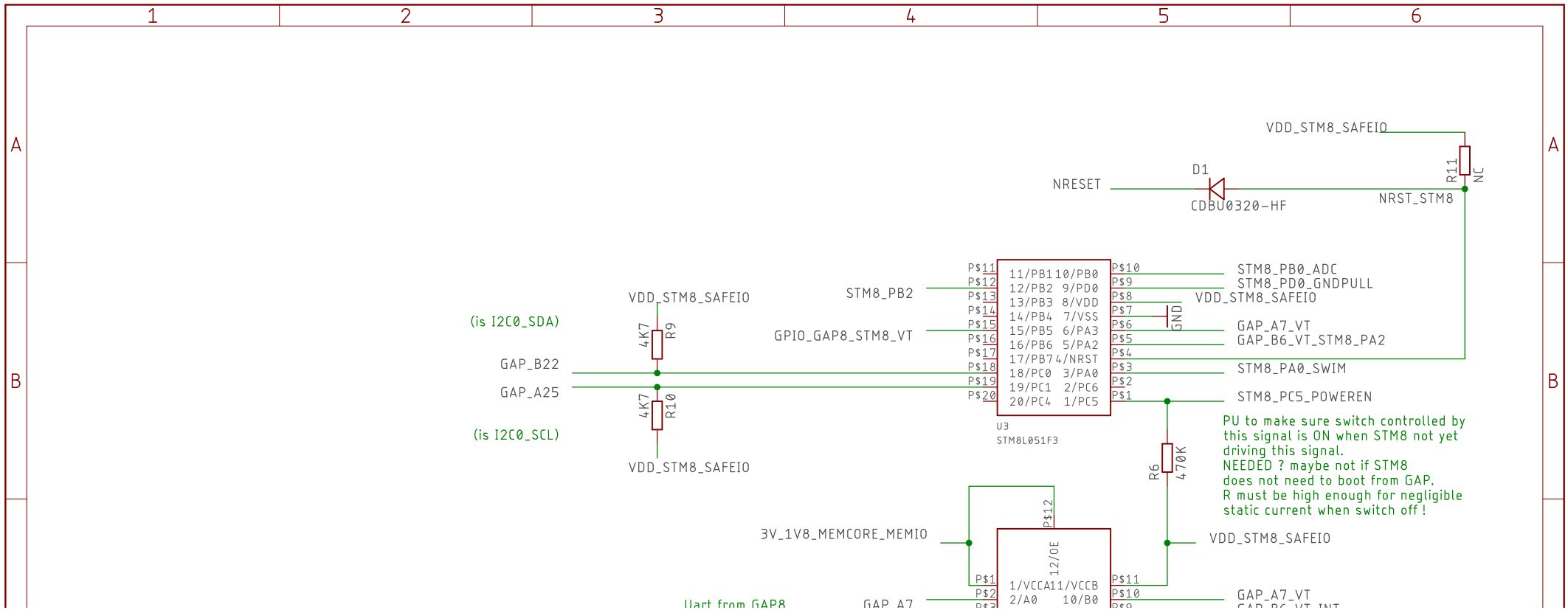
1
2
3
4
5
6
A
B
VDD_STM8_SAFEIO
R11
NC
D1
NRESET
CDBU0320-HF
NRST_STM8
STM8_PB2
GPIO_GAP8_STM8_VT
P$11
P$12
P$13
P$14
P$15
P$16
P$17
P$18
P$19
P$20
11/PB1 10/PB0
12/PB2 9/PD0
13/PB3 8/VDD
14/PB4 7/VSS
15/PB5 6/PA3
16/PB6 5/PA2
17/PB7 4/NRST
18/PC0 3/PA0
19/PC1 2/PC6
20/PC4 1/PC5
P$10
P$9
P$8
P$7
P$6
P$5
P$4
P$3
P$2
P$1
STM8_PB0_ADC
STM8_PD0_GNDPULL
VDD_STM8_SAFEIO
GND
GAP_A7_VT
GAP_B6_VT_STM8_PA2
STM8_PA0_SWIM
STM8_PC5_POWEREN
U3
STM8L051F3
VDD_STM8_SAFEIO
(is I2C0_SDA)
4K7
R9
GAP_B22
GAP_A25
4K7
R10
(is I2C0_SCL)
VDD_STM8_SAFEIO
R6
470K
PU to make sure switch controlled by
this signal is ON when STM8 not yet
driving this signal.
NEEDED ? maybe not if STM8
does not need to boot from GAP.
R must be high enough for negligible
static current when switch off !
3V_1V8_MEMCORE_MEMIO
P$12
12/OE
P$1
P$2
1/VCCA 11/VCCB
2/A0 10/B0
P$11
P$10
VDD_STM8_SAFEIO
GAP_A7_VT
Uart from GAP8
GAP_A7